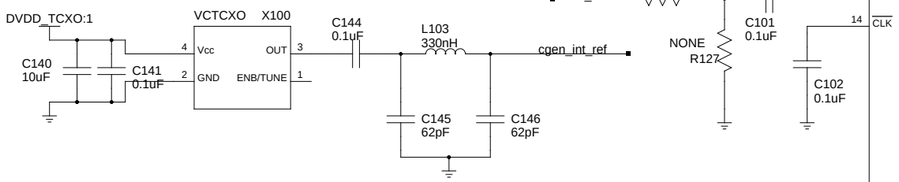
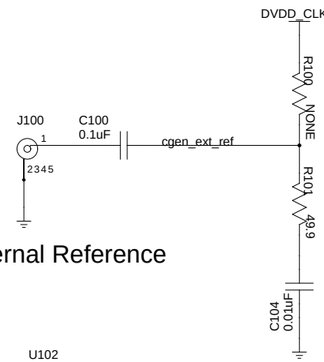
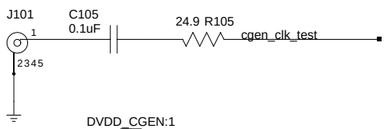
TCXO Internal Reference

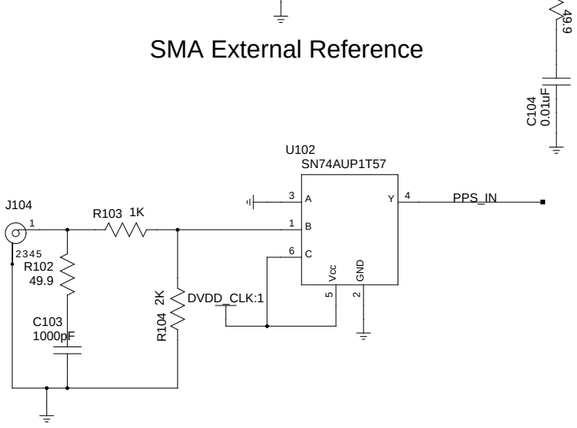


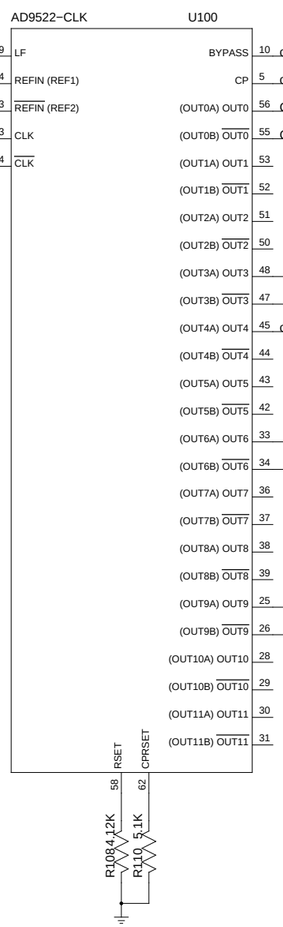
SMA External Reference

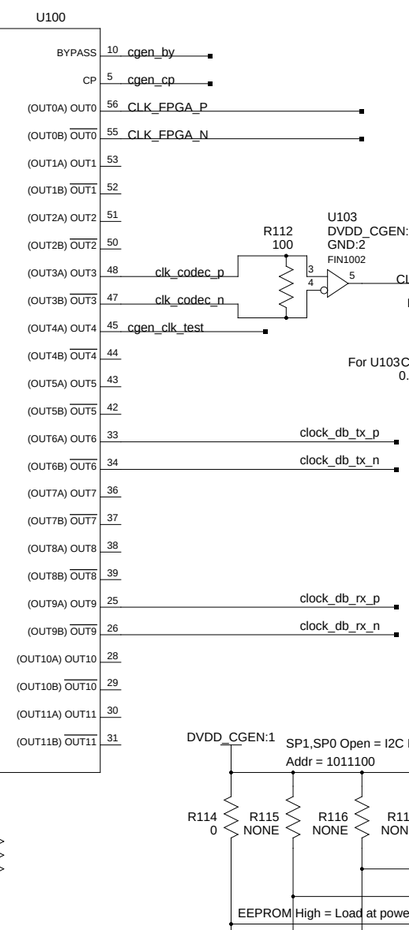


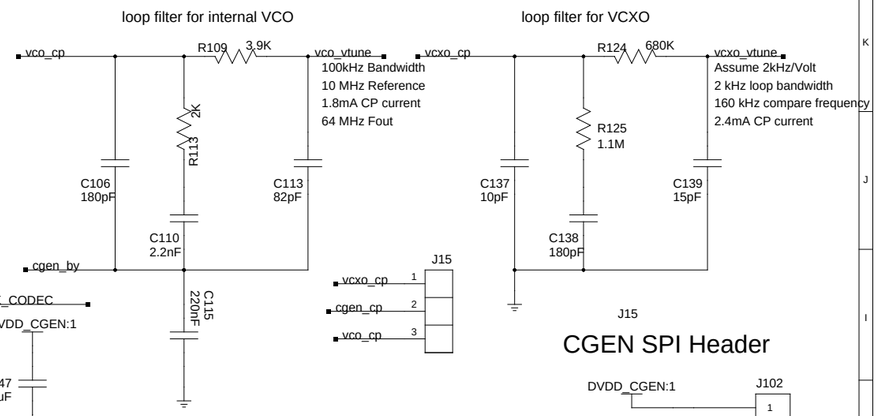
SMA Test Output



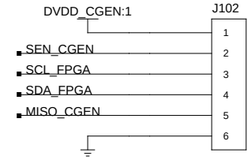


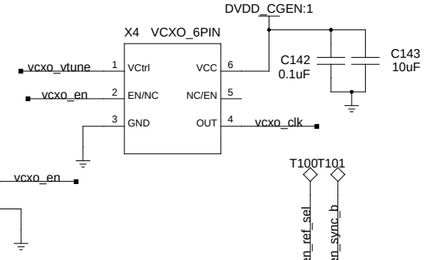


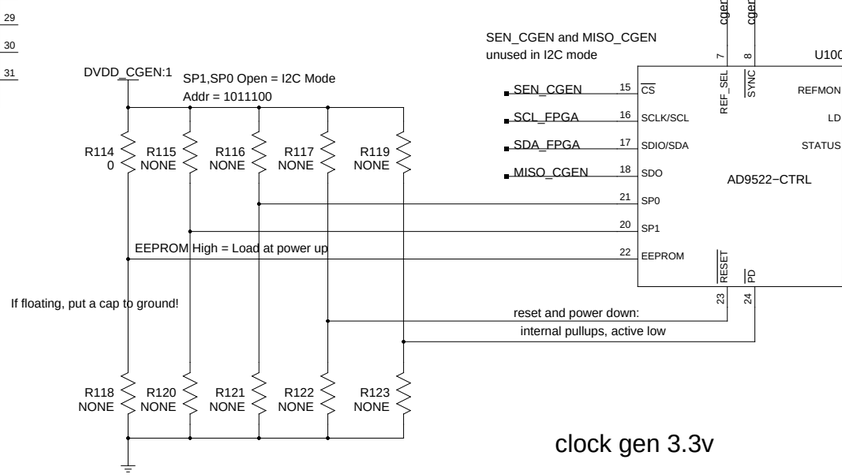


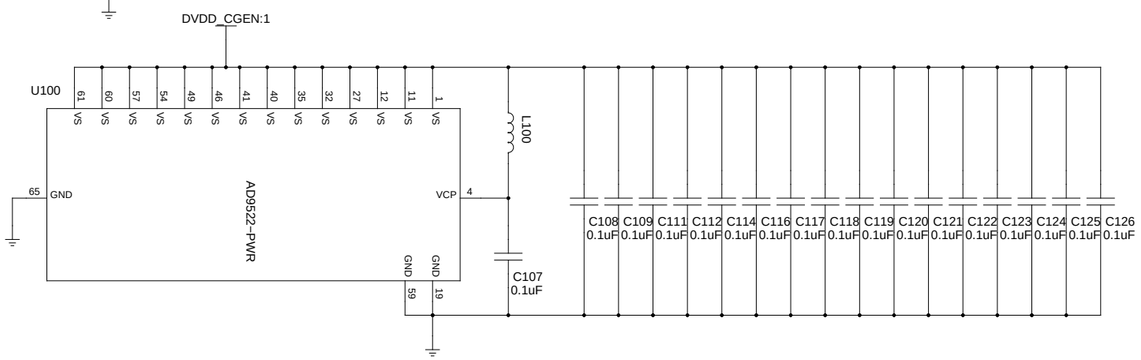


CGEN SPI Header

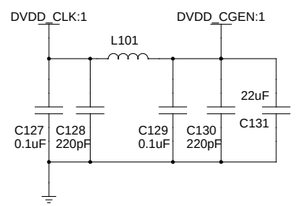




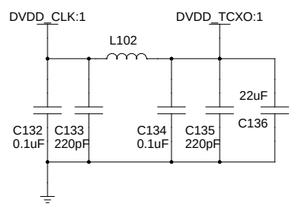




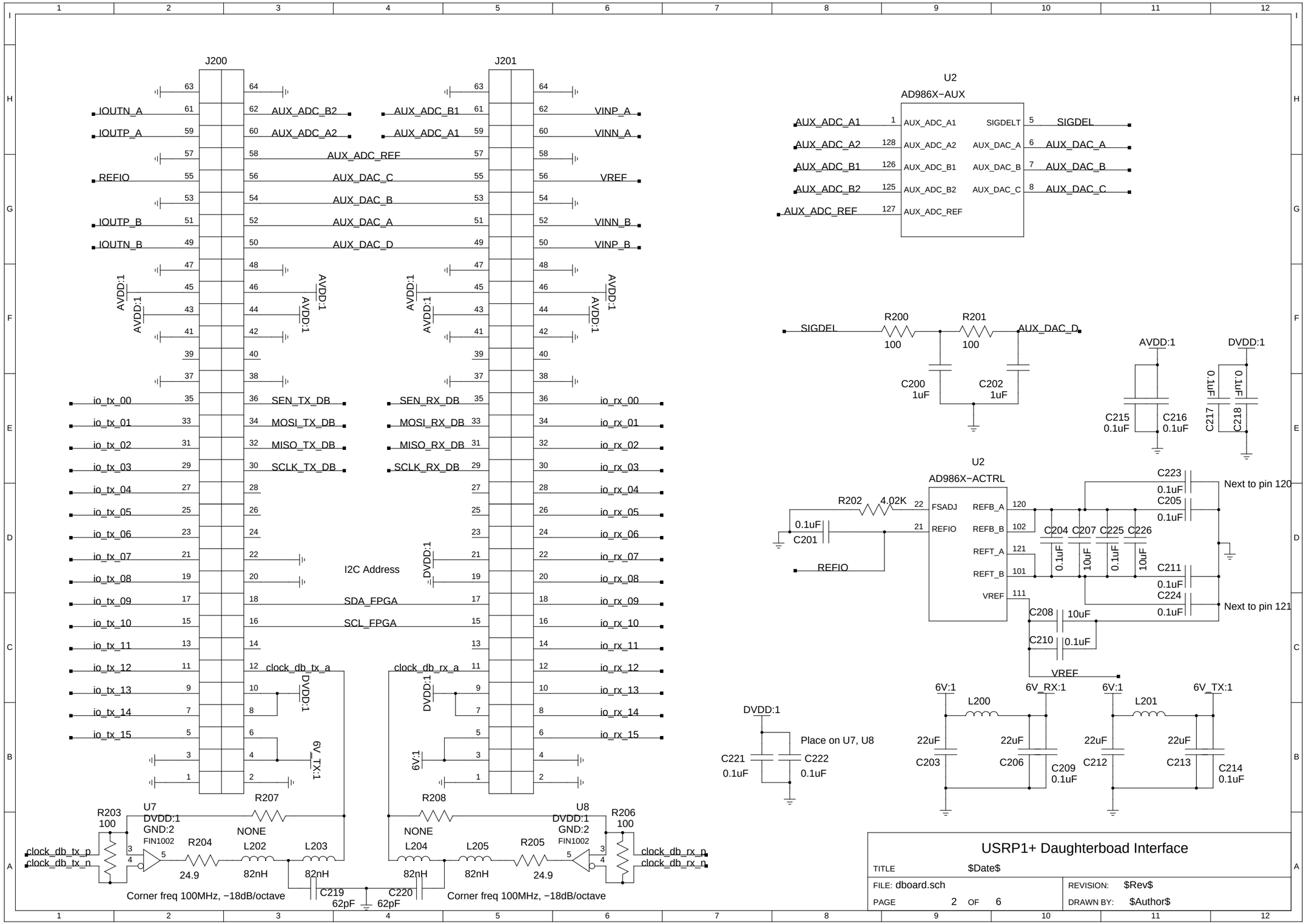
clock gen 3.3v



tcxo 3.3v

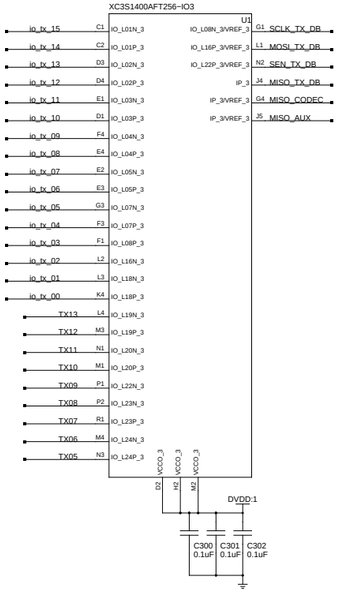


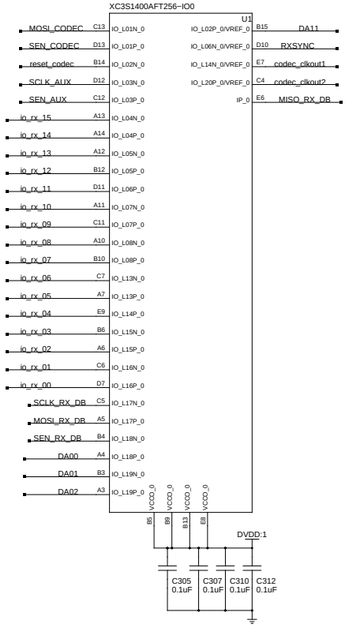
USRP1+ Clock Generation		
TITLE	$Date$	
FILE: clock.sch	REVISION: Rev	
PAGE 1 OF 6	DRAWN BY: $Author$	

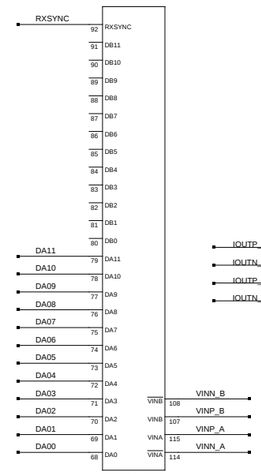


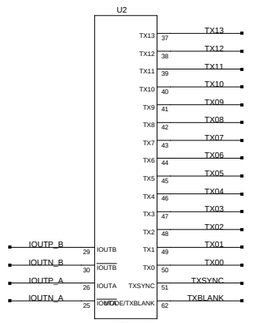
USRP1+ Daughterboad Interface

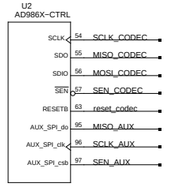
TITLE	$Date$		
FILE: dboard.sch		REVISION:	Rev
PAGE	2 OF 6	DRAWN BY:	$Author$

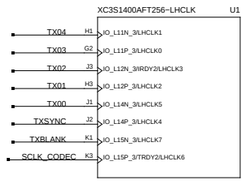


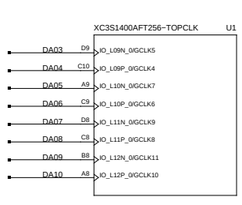


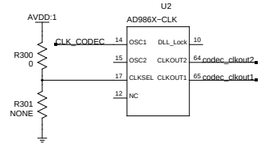


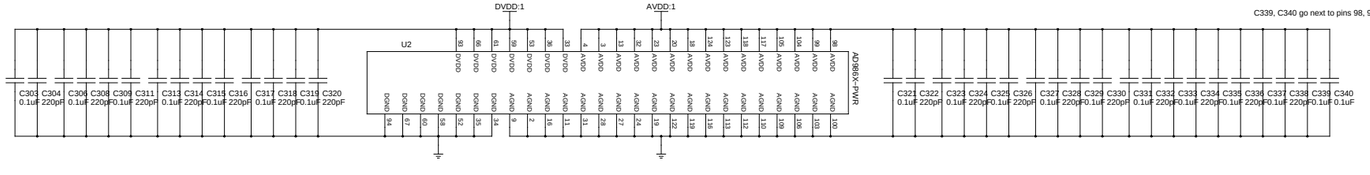












USRP1+ CODEC Interface

TITLE: $Date$			
FILE: fpga_codec.sch	PAGE 3 OF 6	REVISION: Rev	DRAWN BY: $Author$

U1 XC3S1400AFT256-RHCLK

IO_L11N_1/RHCLK1	K14	debug_clk1
IO_L11P_1/RHCLK0	K15	debug_clk0
IO_L12N_1/TRDY1/RHCLK3	J16	debug_01
IO_L12P_1/RHCLK2	K16	debug_00
IO_L15N_1/RHCLK7	H16	gpif_adr1
IO_L15P_1/IRDY1/RHCLK6	H15	cgen_sync_b

XC3S1400AFT256-IO1

U1

debug_31	N14	IO_L01N_1/LDC2	IP_1/VREF_1	H12	
debug_30	N13	IO_L01P_1/HDC	IP_1/VREF_1	J14	cgen_st_refmon
debug_29	P15	IO_L02N_1/LDC0	IP_1/VREF_1	M13	cgen_st_ld
debug_28	R15	IO_L02P_1/LDC1	IP_1/VREF_1	M14	PPS_IN
debug_27	N16	IO_L03N_1/A1			
debug_26	P16	IO_L03P_1/A0			
debug_25	K13	IO_L06N_1/A3			
debug_24	L13	IO_L06P_1/A2			
debug_23	M16	IO_L07N_1/A5			
debug_22	M15	IO_L07P_1/A4			
debug_21	L16	IO_L08N_1/A7			
debug_20	L14	IO_L08P_1/A6			
debug_19	J13	IO_L10N_1/A9			
debug_18	J12	IO_L10P_1/A8			
debug_17	F16	IO_L16N_1/A11			
debug_16	G16	IO_L16P_1/A10			
debug_15	G14	IO_L17N_1/A13			
debug_14	H13	IO_L17P_1/A12			
debug_13	F15	IO_L18N_1/A15			
debug_12	E16	IO_L18P_1/A14			
debug_11	F14	IO_L19N_1/A17			
debug_10	G13	IO_L19P_1/A16			
debug_09	F13	IO_L20N_1/A19			
debug_08	E14	IO_L20P_1/A18			
debug_07	D15	IO_L22N_1/A21			
debug_06	D16	IO_L22P_1/A20			
debug_05	D14	IO_L23N_1/A23			
debug_04	E13	IO_L23P_1/A22			
debug_03	C15	IO_L24N_1/A25			
debug_02	C16	IO_L24P_1/A24			

VCCO_1 E15, VCCO_1 J15, VCCO_1 N15

DVDD:1

C408 0.1uF, C409 0.1uF, C410 0.1uF

debug connector

J402

MICTOR43-LA

debug_clk0	5	CLK0	CLK1	6	debug_clk1
debug_31	7	A3[7]	A1[7]	8	debug_15
debug_30	9	A3[6]	A1[6]	10	debug_14
debug_29	11	A3[5]	A1[5]	12	debug_13
debug_28	13	A3[4]	A1[4]	14	debug_12
debug_27	15	A3[3]	A1[3]	16	debug_11
debug_26	17	A3[2]	A1[2]	18	debug_10
debug_25	19	A3[1]	A1[1]	20	debug_09
debug_24	21	A3[0]	A1[0]	22	debug_08
debug_23	23	A2[7]	A0[7]	24	debug_07
debug_22	25	A2[6]	A0[6]	26	debug_06
debug_21	27	A2[5]	A0[5]	28	debug_05
debug_20	29	A2[4]	A0[4]	30	debug_04
debug_19	31	A2[3]	A0[3]	32	debug_03
debug_18	33	A2[2]	A0[2]	34	debug_02
debug_17	35	A2[1]	A0[1]	36	debug_01
debug_16	37	A2[0]	A0[0]	38	debug_00

GND 39, GND 40, GND 41, GND 42, GND 43, NC 1, NC 2, NC 3, NC 4

TITLE	USRP1+ Debug and Misc
	$Date$
FILE: fpga_debug.sch	REVISION: Rev
PAGE 4 OF 6	DRAWN BY: $Author$

CY7C68013−TQ100−BUS

GPIF_CTL0 54 CTL0
GPIF_CTL1 55 CTL1
GPIF_CTL2 56 CTL2
GPIF_CTL3 51 CTL3
52 CTL4
76 CTL5
GPIF_RDY0 3 RDY0
GPIF_RDY1 4 RDY1
GPIF_RDY2 5 RDY2
GPIF_RDY3 6 RDY3
7 RDY4
8 RDY5
GPIF_D00 34 FD0
GPIF_D01 35 FD1
GPIF_D02 36 FD2
GPIF_D03 37 FD3
GPIF_D04 44 FD4
GPIF_D05 45 FD5
GPIF_D06 46 FD6
GPIF_D07 47 FD7
GPIF_D08 80 FD8
GPIF_D09 81 FD9
GPIF_D10 82 FD10
GPIF_D11 83 FD11
GPIF_D12 95 FD12
GPIF_D13 96 FD13
GPIF_D14 97 FD14
GPIF_D15 98 FD15

U3

Connect others to header

IFCLK 26 IFCLK

DVDD_CYP:1

1K R540 1K R541

D508 D509

U3 CY7C68013−TQ100−PE

PE0/T0OUT 86
PE1/T1OUT 87
PE2/T2OUT 88
PE3/RXD0OUT 89
PE4/RXD1OUT 90
PE5/INT6 91
PE6/T2EX 92
PE7/GPIFADR8 93

U3 CY7C68013−TQ100−PC

PC0 57
PC1 58
PC2 59 fx2_wakeup
PC3 60
PC4 61
PC5 62
PC6 63 fpga_cfg_init_b
PC7 64 fpga_cfg_done

LED1 slot=2 R500 1K DVDD:1

K2 A2 Q500 fpga_cfg_done R501 4.7K

LED1 slot=3 R502 1K

K3 A3 Q501 fpga_cfg_init_b R503 4.7K

U3 CY7C68013−TQ100−PA

PA0/INT0 67 fpga_cfg_cclk
PA1/INT1 68 fpga_cfg_prog_b
PA2/SLOE 69 gpif_sloe
PA3/WU2 70 fpga_cfg_din
PA4/FIFOADR0 71 gpif_adr0
PA5/FIFOADR1 72 gpif_adr1
PA6/PKTEND 73 gpif_pktend
PA7/FLAGD/SLCS 74 gpif_cs

DVDD:1

2.2K R509 2.2K R513

SCL_FX2 R506 49.9 SCL_FPGA
SDA_FX2 49.9 R511 SDA_FPGA

DVDD_CYP:1

2.2K R504 2.2K R505

U500 24Cxx

A0 A1 A2 n/c SCL SDA

24LC024/SN
DVDD_CYP:8
GND:4

U3 CY7C68013−TQ100−MISC

SCL 29
SDA 30
TxD0 40
RxD0 41
TxD1 42
RxD1 43
NC 13
NC 14
NC 15
INT4 22
INT5 84
T0 23
T1 24
T2 25

U1 XC3S1400AFT256−CFG

R507 NONE debug_led0 P4 IO_L01N_2/M0
R508 NONE debug_led1 N4 IO_L01P_2/M1
cgen_ref_sel T2 IO_L02N_2/CSO_B
R512 NONE debug_led2 R2 IO_L02P_2/M2
GPIF_D08 T3 IO_L03N_2/VS2
GPIF_D09 R3 IO_L03P_2/RDWR_B
GPIF_D10 P5 IO_L04N_2/VS0
GPIF_D11 N6 IO_L04P_2/VS1
GPIF_D12 T6 IO_L06N_2/D6
GPIF_D13 T5 IO_L06P_2/D7
GPIF_D14 N8 IO_L08N_2/D4
GPIF_D15 P7 IO_L08P_2/D5
gpif_pktend P10 IO_L14N_2/MOSI/CSI_B
gpif_sloe R11 IO_L15N_2/DOUT
gpif_adr0 T11 IO_L15P_2/AWAKE
gpif_cs P12 IO_L17N_2/D3
fpga_cfg_init_b T12 IO_L17P_2/INIT_B
SCL_FPGA R13 IO_L18N_2/D1
SDA_FPGA T13 IO_L18P_2/D2
fpga_cfg_cclk R14 IO_L20N_2/CCLK
fpga_cfg_din T14 IO_L20P_2/D0/DIN/MISO
IO_L20N_0/PUDC_B D5 reset_n

R523 1K DVDD:1

R521 4.7K S501

SUSPEND R16
PROG_B A2
DONE T15

fpga_cfg_prog_b
fpga_cfg_done

pullups enabled
m[0:2] = 1
serial slave

debug leds 0−2

DVDD:1

LED2 slot=3 R515 1K

K3 A3 Q502 debug_led2 R516 4.7K

LED2 slot=2 R517 1K

K2 A2 Q503 debug_led1 R518 4.7K

LED2 slot=1 R520 1K

K1 A1 Q504 debug_led0 R522 4.7K

XC3S1400AFT256−BOTCLK U1

CLK_FPGA_N T7 IO_L09N_2/GCLK13
CLK_FPGA_P R7 IO_L09P_2/GCLK12
IFCLK T8 IO_L10N_2/GCLK15
GPIF_D00 P8 IO_L10P_2/GCLK14
GPIF_D01 P9 IO_L11N_2/GCLK1
GPIF_D02 N9 IO_L11P_2/GCLK0
GPIF_D03 T9 IO_L12N_2/GCLK3
GPIF_D04 R9 IO_L12P_2/GCLK2

DVDD_CYP:1

U501

VCC 5
P3 14
P4 2
CLK 3
VSS 11
SCL 12 SCL_FX2
SDA 13 SDA_FX2
RES 4 AUTH_RSET

R5H30211

R531 100K
R532 10K

Secure Auth Chip

C500 PESD0402−140
C501 PESD0402−140

J500 4 3 2 1

U3 CY7C68013−TQ100−CTRL

CLKOUT 100
D+ 17
D− 18
XTALIN 11
XTALOUT 10
BKPT 28
RD 31
RESERVED 27
RESET 77
WAKEUP 79
WR 32

DVDD_CYP:1

R519 100K

C510 0.1uF

S500

30K R514 fx2_wakeup

C503 0.1uF

R510 60.4K

X3

C506 22pF C507 22pF

fx2_wakeup

J501 XIL−PLAT−CABLE

GND 1 Vref/Vref 2
GND 3 PROG/TMS 4
GND 5 CCLK/TCK 6
GND 7 Done/TDO 8
GND 9 Din/TDI 10
GND 11 NC/NC 12
GND 13 INIT/NC 14

DVDD:1

R524 10 TCK
R525 10 TDI
R527 10 TDO
R529 10 TMS

R526 10K R528 10K R530 10K

XC3S1400AFT256−JTAG U1

TCK A15
TDI B1
TDO B16
TMS B2

fx2/cypress 3.3v

DVDD:1 L501 DVDD_CYP:1

C521 0.1uF C522 220pF C523 0.1uF C524 220pF C525 22uF

XC3S1400AFT256−IO2 U1

GPIF_RDY0 R5 IO_L05N_2
GPIF_RDY1 T4 IO_L05P_2
GPIF_RDY2 T10 IO_L14P_2
GPIF_RDY3 N11 IO_L16N_2
GPIF_D05 P11 IO_L16P_2
GPIF_D06 P13 IO_L19N_2
GPIF_D07 N12 IO_L19P_2

IP_2/VREF_2 M7 GPIF_CTL0
IP_2/VREF_2 M9 GPIF_CTL1
IP_2/VREF_2 M11 GPIF_CTL2
IP_2/VREF_2 N5 GPIF_CTL3
IP_2/VREF_2 P6 cgen_st_status

VCCO_2 R4 R8 R12

DVDD:1

C502 0.1uF C504 0.1uF C505 0.1uF

DVDD_CYP:1

L500

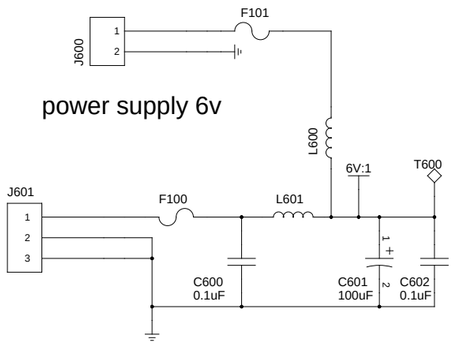
U3 CY7C68013−TQ100−PWR

VCC 85 78 66 53 49 38 33 20 16 1
AVCC 9
GND 99 94 75 65 50 48 39 21 19 2
AGND 12

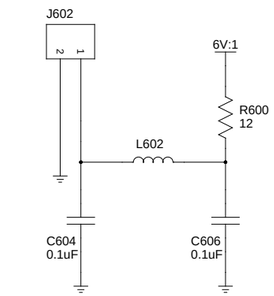
C508 C509 0.1uF 220pF
C511 C512 0.1uF 220pF
C513 C514 0.1uF 220pF
C515 C516 0.1uF 220pF
C517 C518 0.1uF 220pF
C519 C520 0.1uF 220pF

USRP1+ FX2	
TITLE: $Date$	
FILE: fpga_fx2.sch	REVISION: Rev
PAGE 5 OF 6	DRAWN BY: $Author$

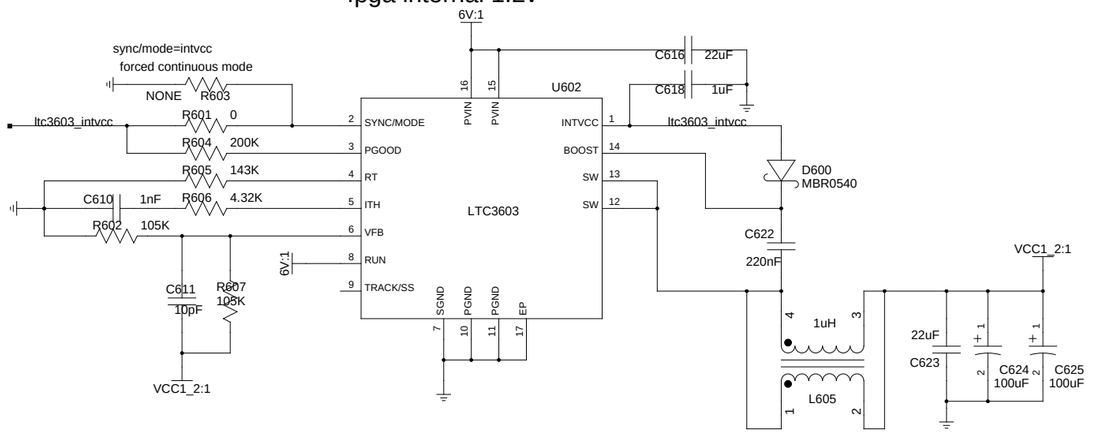
power supply 6v

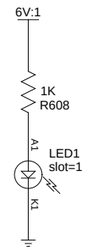


fan connector 6v

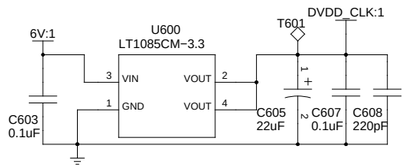


fpga internal 1.2v

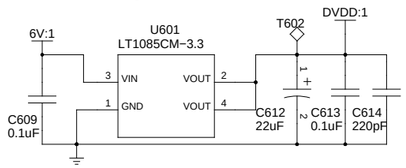




clock 3.3v



digital 3.3v



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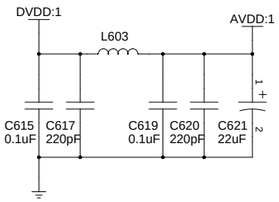

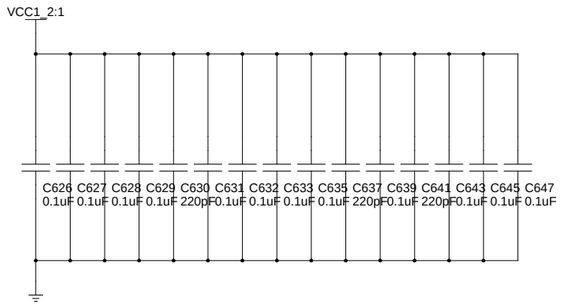

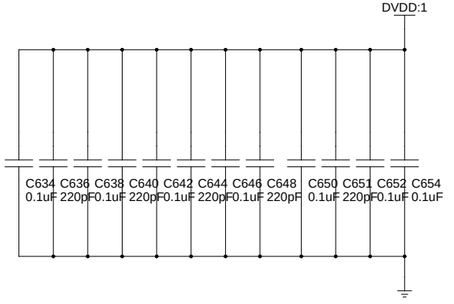

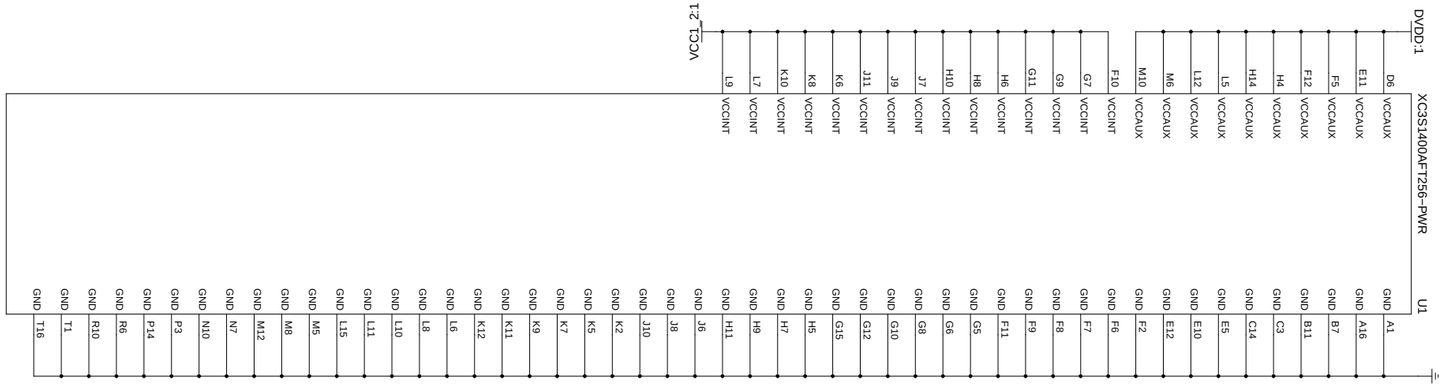

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