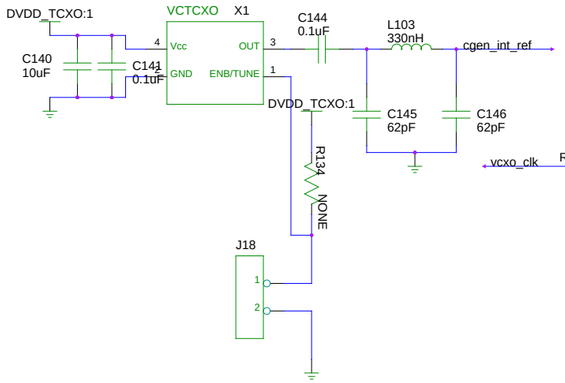
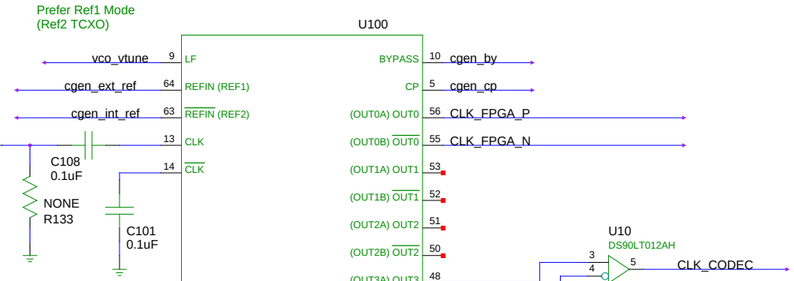
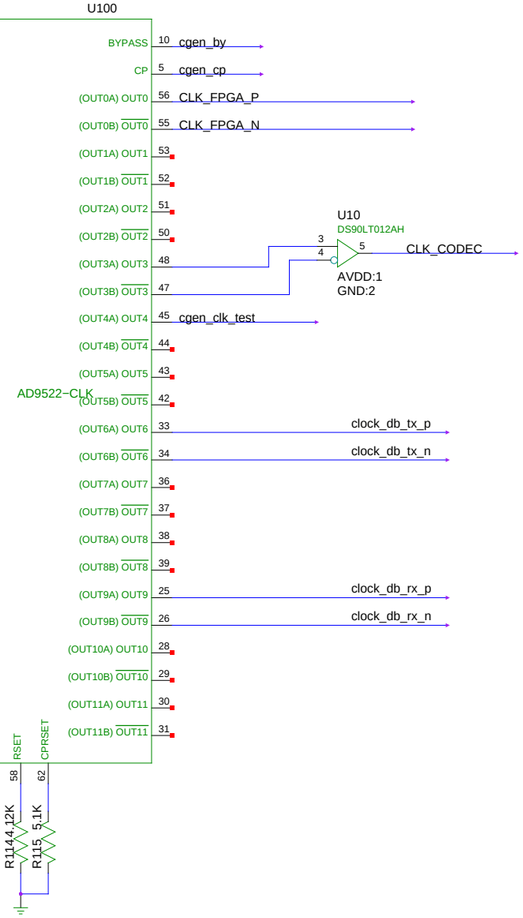
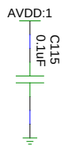
TCXO Internal Reference

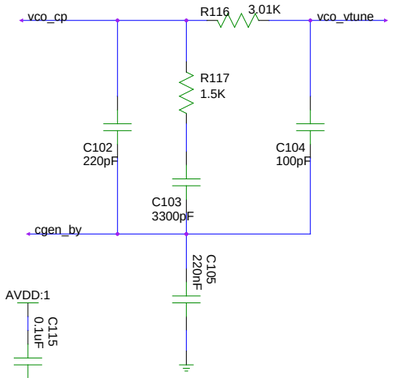




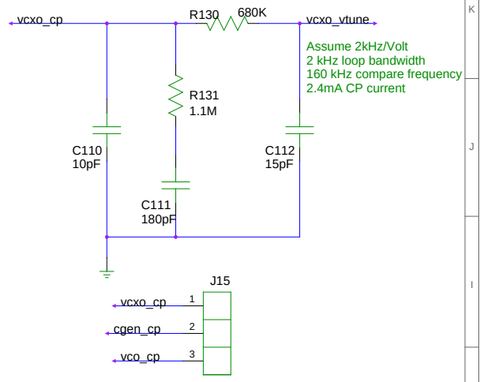




loop filter for internal VCO

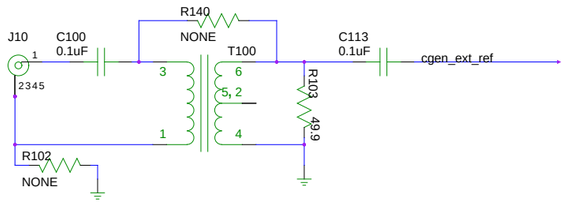


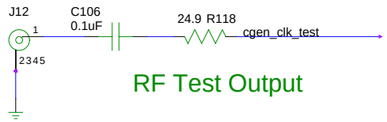
loop filter for VCXO



Assume 2kHz/Volt
2 kHz loop bandwidth
160 kHz compare frequency
2.4mA CP current

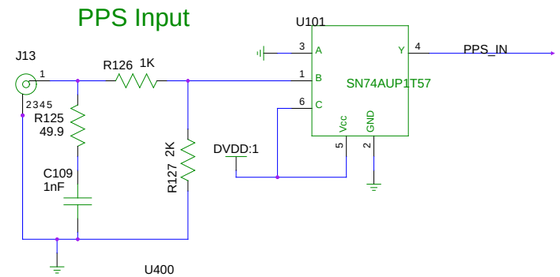
10MHz External Reference

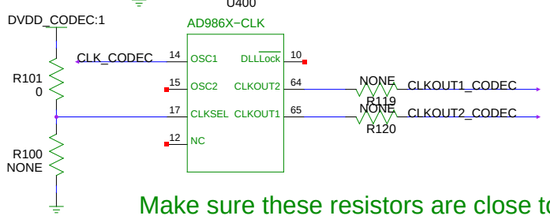




RF Test Output

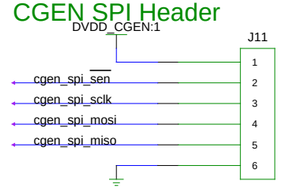
PPS Input

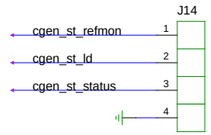


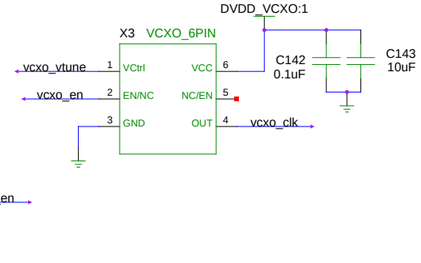


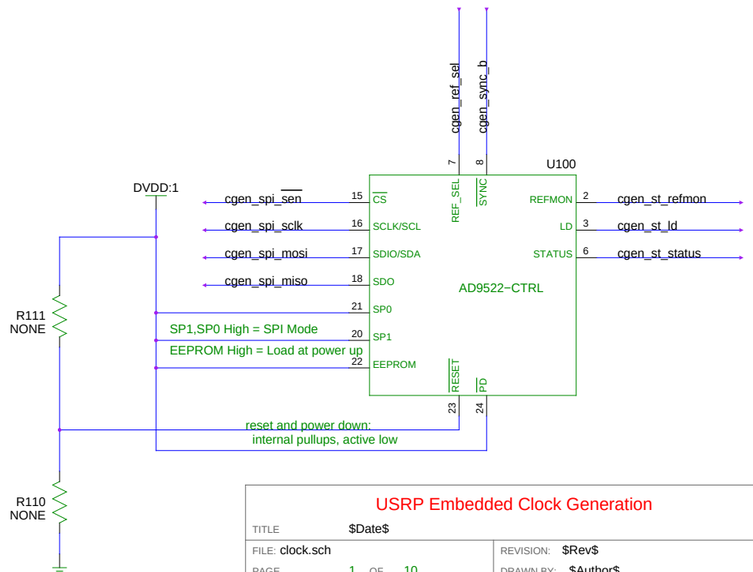
Make sure these resistors are close to U400

CGEN SPI Header



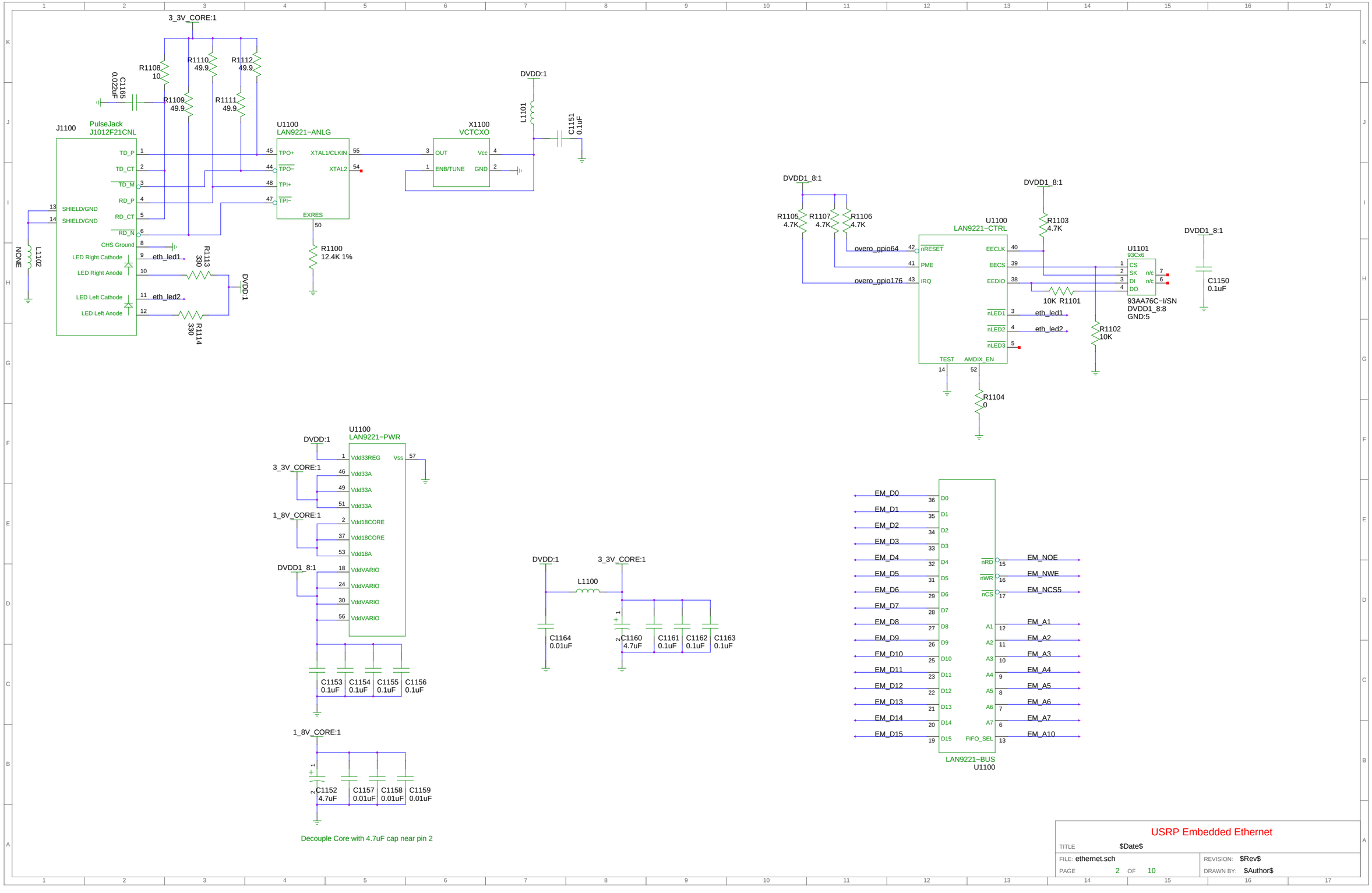






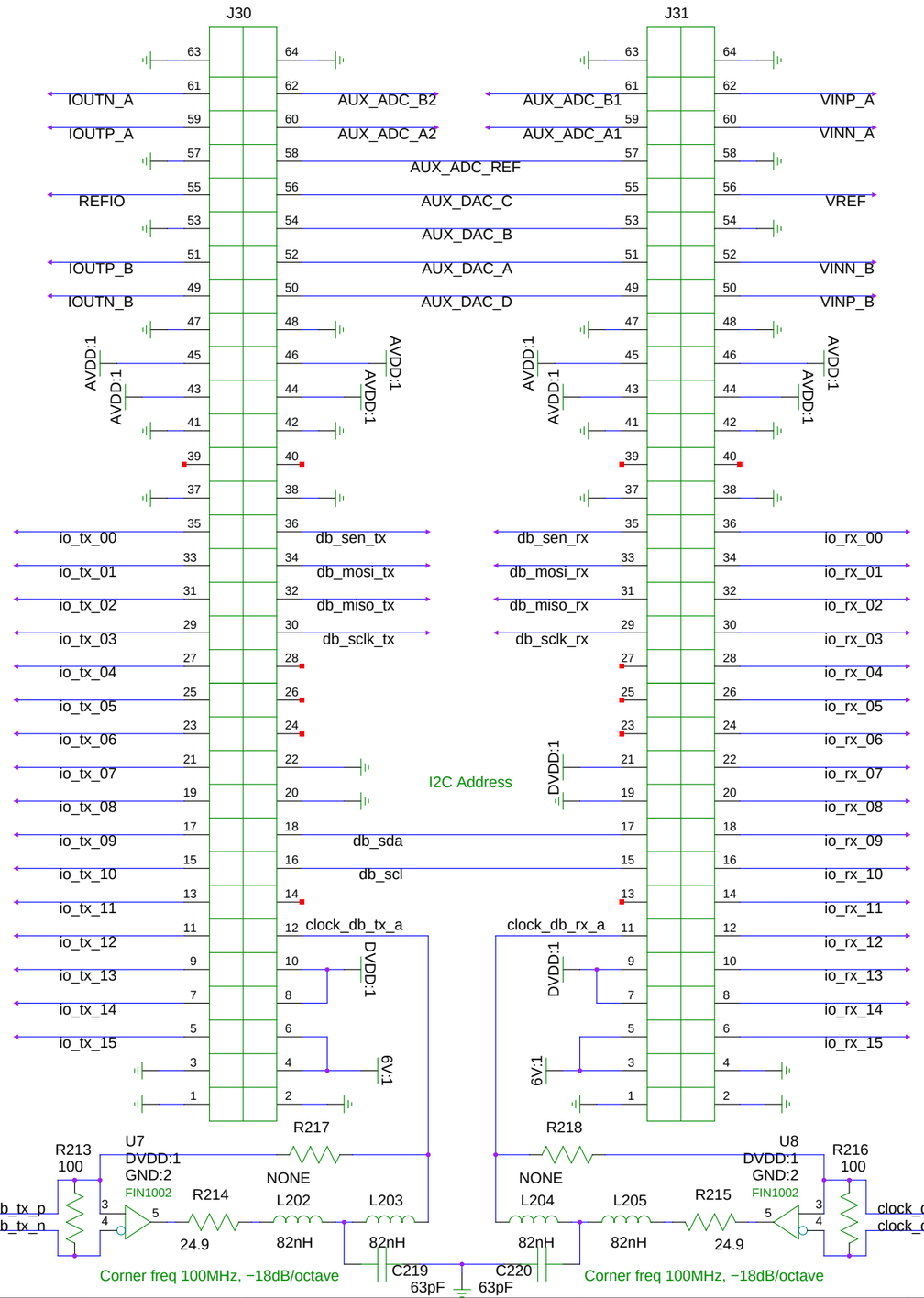
USRP Embedded Clock Generation

TITLE	$Date$
FILE: clock.sch	REVISION: Rev
PAGE 1 OF 10	DRAWN BY: $Author$



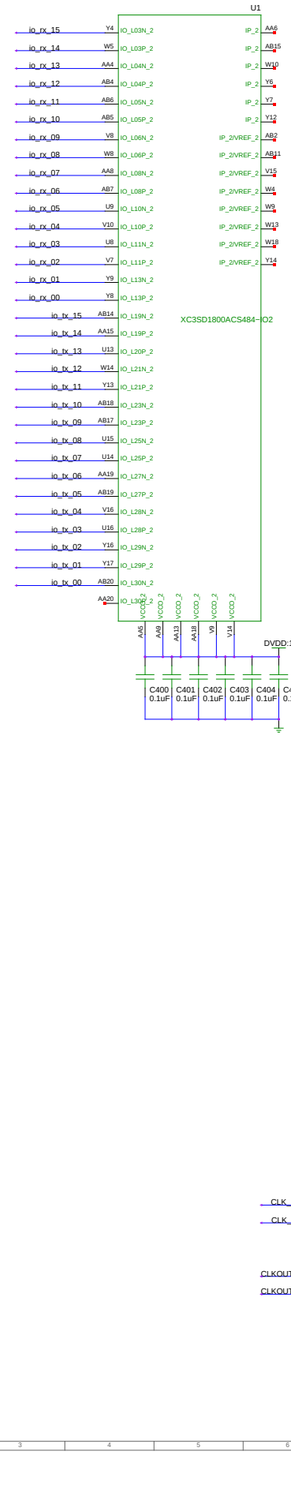
USRP Embedded Ethernet

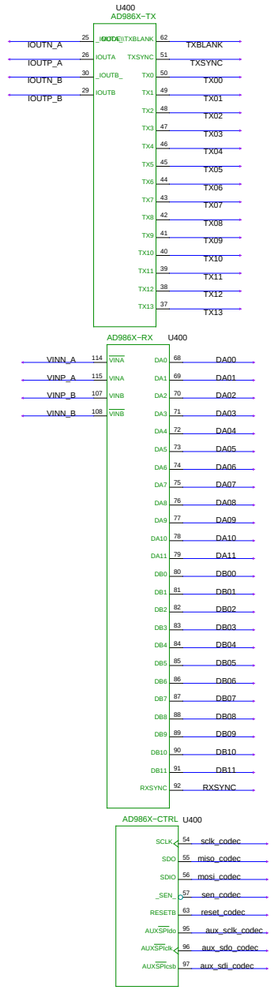
TITLE	$Date$		
FILE: ethernet.sch		REVISION:	Rev
PAGE 2 OF 10		DRAWN BY:	$Author$

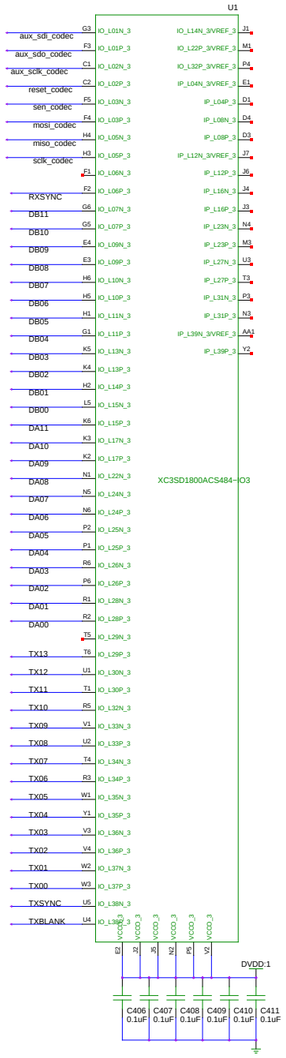


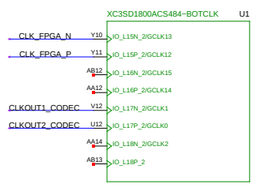
USRP Embedded Daughterboad Interface

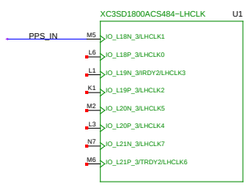
TITLE	$Date$		
FILE: dboard.sch		REVISION:	Rev
PAGE	3 OF 10	DRAWN BY:	$Author$











USRP Embedded FPGA and CODECs

TITLE	$Date$		
FILE: fpga_codec.sch	PAGE 4 OF 10	REVISION: Rev	DRAWN BY: $Author$

convert fpga config outputs

convert fpga config inputs

LED1 slot=3 — debug_led3 — K3 — A3 — R510 1K — DVDD:1

LED1 slot=2 — fpga_cfg_done — A2 — K2 — R509 1K

DVDD1_8:1 — 4.7K R200 — overo_cfg_done_b — Q20 — 4.7K R201 — DVDD:1 — fpga_cfg_done

DVDD1_8:1 — 4.7K R202 — overo_cfg_init — Q21 — 4.7K R203 — DVDD:1 — fpga_cfg_init_b

U201 SN74AUP1T57: overo_cfg_din → fpga_cfg_din; 0 R209, NONE R206; Vcc DVDD:1, GND

U202 SN74AUP1T57: overo_cfg_cclk → fpga_cfg_cclk; 0 R208, NONE R205; Vcc DVDD:1, GND

U203 SN74AUP1T57: overo_cfg_prog_b → fpga_cfg_prog_b; 0 R207, NONE R204; Vcc DVDD:1, GND

DVDD1_8:1 — 4.7K R210

U1 XC3SD1800ACS484-CFG

F7 IO_L31N_0/PUDC_B — R511 0

pullups enabled
m[0:2] = 1
serial slave

IO_L01N_2/M0	AB3	NONE R512
IO_L01P_2/M1	AA3	NONE R513
IO_L02N_2/CSO_B	U7	
IO_L02P_2/M2	V6	NONE R514
IO_L07N_2/VS2	W6	
IO_L07P_2/RDWR_B	Y5	
IO_L09N_2/VS0	AB9	fpga_txd1
IO_L09P_2/VS1	AB8	fpga_rxd1
IO_L12N_2/D6	AA10	
IO_L12P_2/D7	AB10	
IO_L14N_2/D4	U10	
IO_L14P_2/D5	V11	
IO_L20N_2/MOSI/CSI_B	V13	
IO_L22N_2/DOUT	AB16	
IO_L24N_2/D3	Y15	debug_led3
IO_L24P_2/INIT_B	W15	fpga_cfg_init_b
IO_L26N_2/D1	Y19	
IO_L26P_2/D2	Y18	
IO_L31N_2/CCLK	V17	fpga_cfg_cclk
IO_L31P_2/D0/DIN/MISO	W17	fpga_cfg_din

DONE — AB21 — fpga_cfg_done

IO_L22P_2/AWAKE — AA17

PROG_B — A2 — fpga_cfg_prog_b

SUSPEND — V19

J50 XIL-PLAT-CABLE

1	GND	Vref/Vref	2
3	GND	PROG/TMS	4 — TMS
5	GND	CCLK/TCK	6 — TCK
7	GND	Done/TDO	8 — TDO
9	GND	Din/TDI	10 — TDI
11	GND	NC/NC	12
13	GND	INIT/NC	14

DVDD:1 — R506 10K, R505 10K, R500 10K

R504 10 — TCK
R501 10 — TDI
R502 10 — TDO
R503 10 — TMS

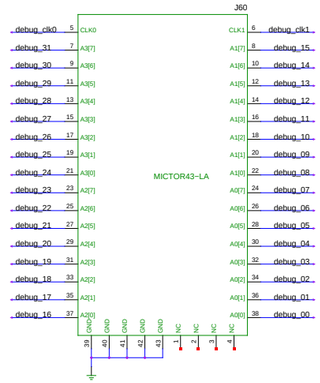
XC3SD1800ACS484-JTAG U1

A21	TCK
D2	TDI
B22	TDO
B1	TMS

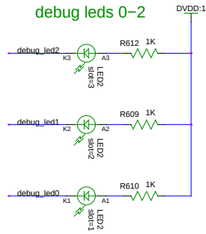
USRP Embedded FPGA Config

TITLE	$Date$		
FILE: fx2.sch		REVISION:	Rev
PAGE	5 OF 10	DRAWN BY:	$Author$

debug connector

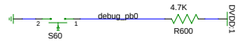


debug leds 0−2

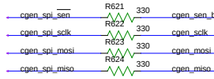


U1

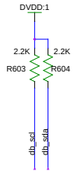
push button



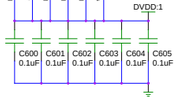
cgen spi



db i2c



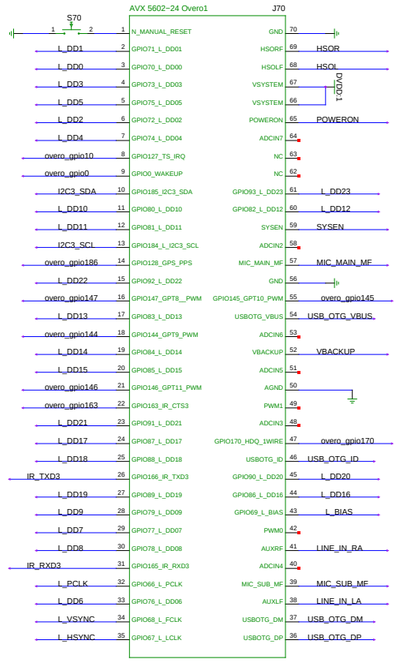
DVDD:1

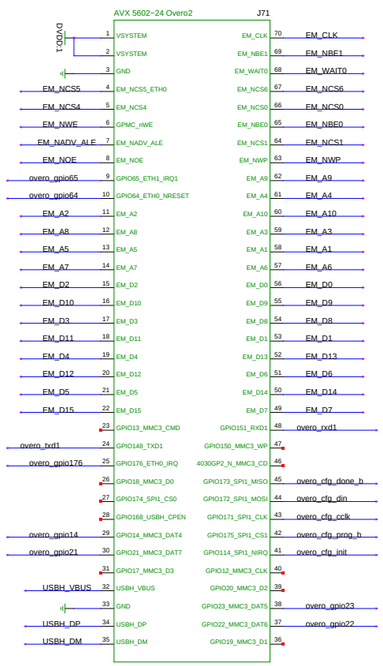


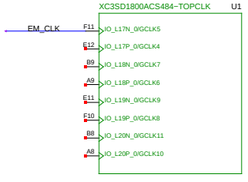
XC3SD1800ACS484-RHCLK

USRP Embedded FPGA and Debug

TITLE:	$Date$		
FILE:	fpga_debug.sch	REVISION:	Rev
PAGE	6 OF 10	DRAWN BY:	$Author$



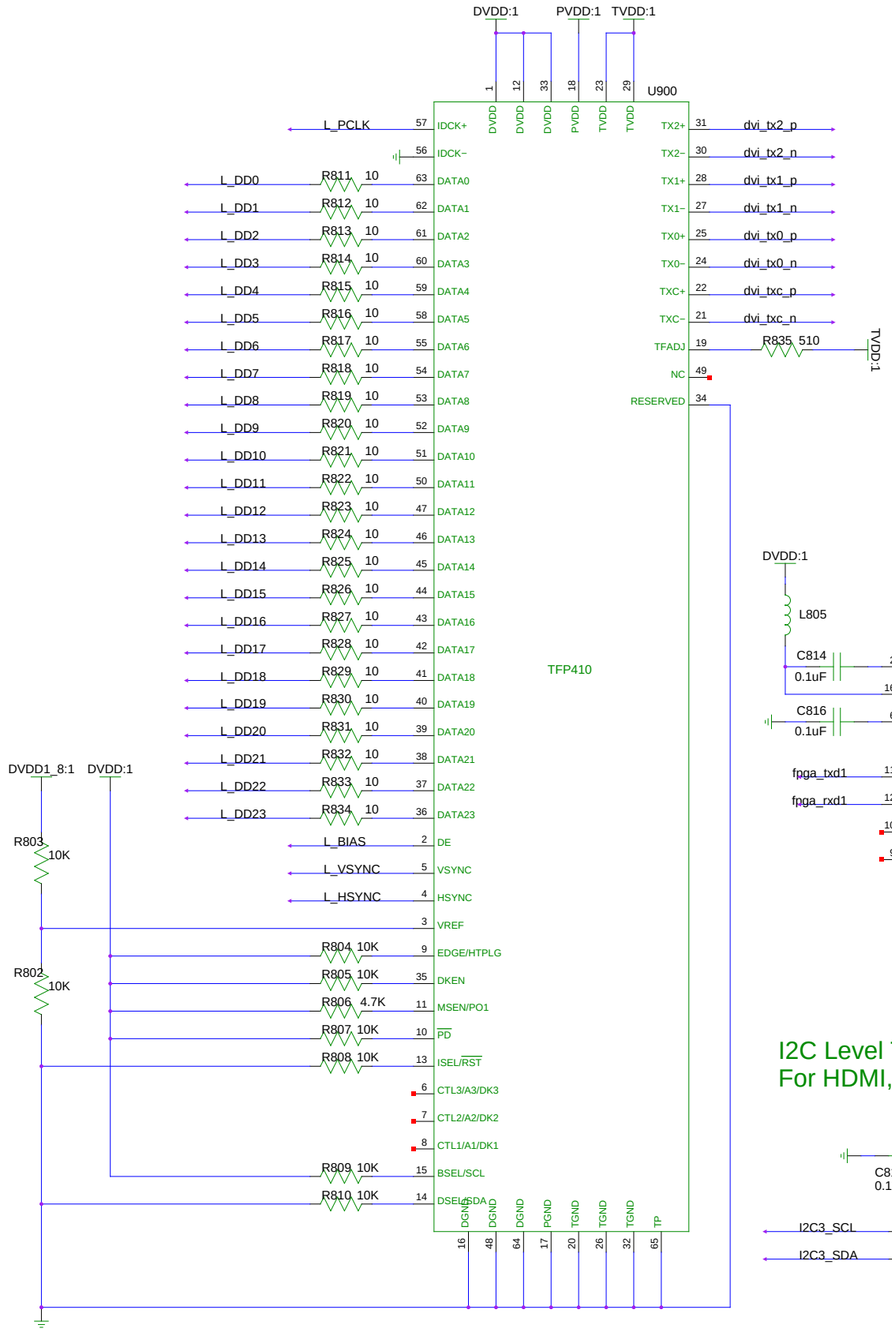




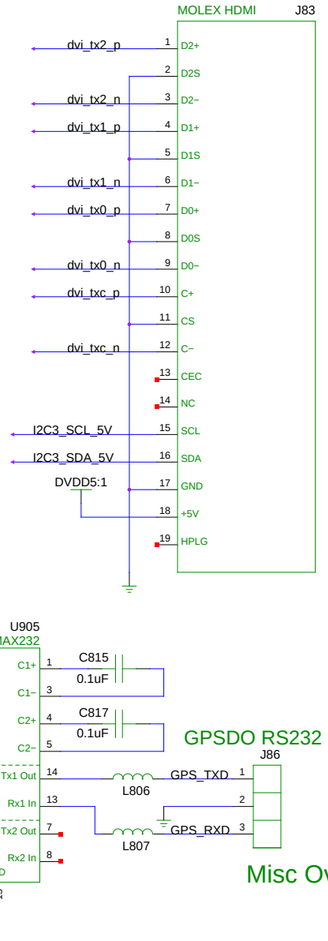
USRP Embedded FPGA and Overo Interface

TITLE: $Date$			
FILE: fpga_overo.sch		REVISION:	Rev
PAGE: 7 OF 10		DRAWN BY:	$Author$

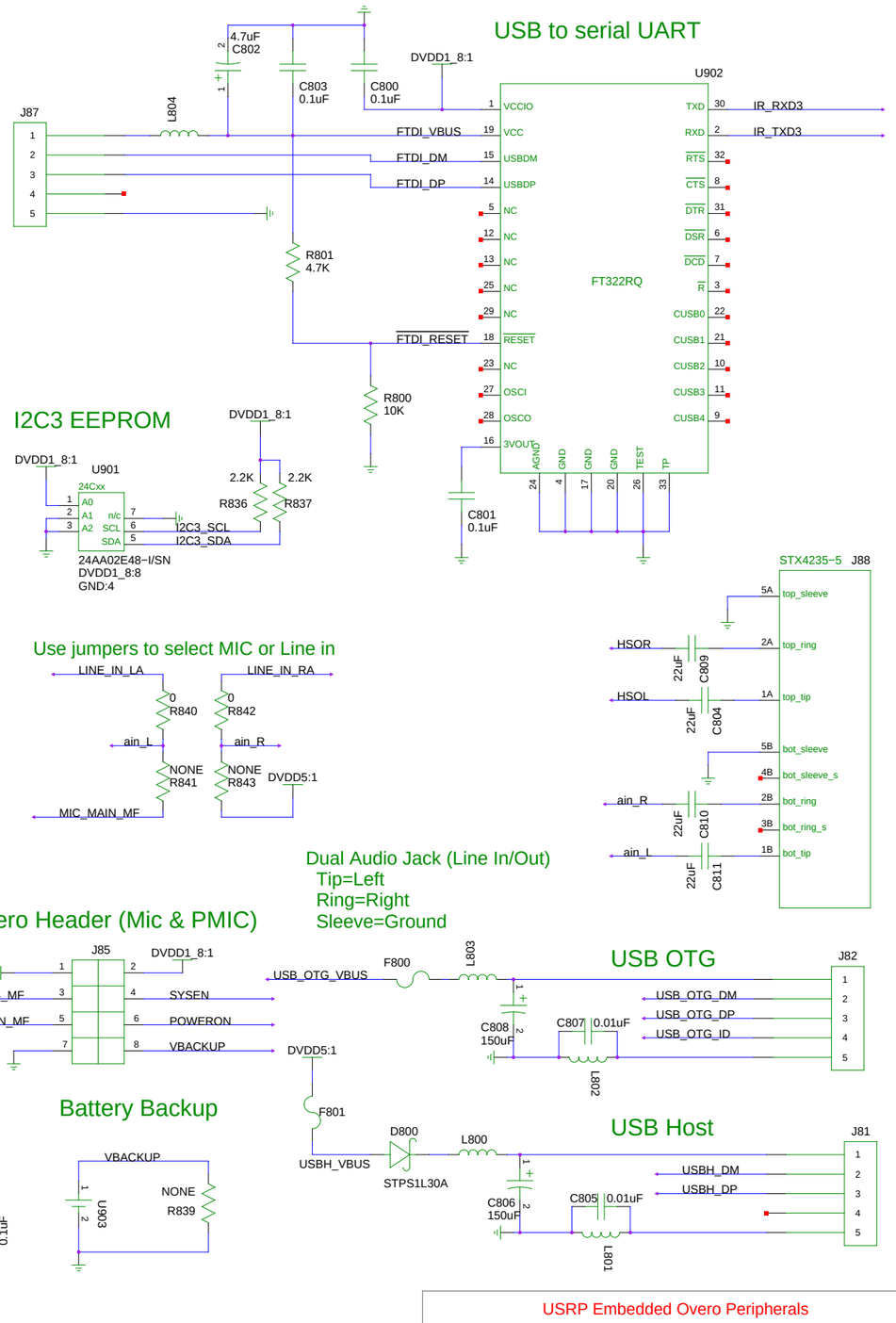
HDMI driver



HDMI connector



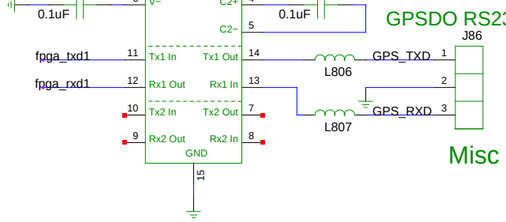
USB to serial UART



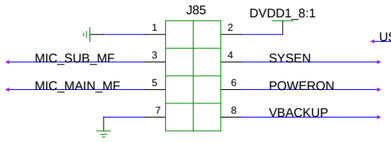
I2C3 EEPROM

Use jumpers to select MIC or Line in

GPSDO RS232



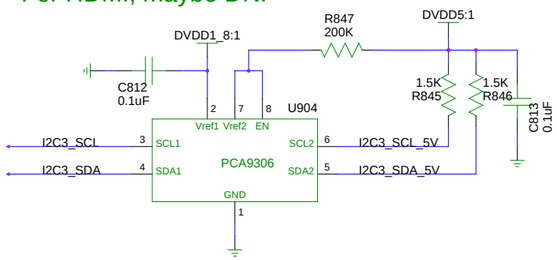
Misc Overo Header (Mic & PMIC)



Dual Audio Jack (Line In/Out)
Tip=Left
Ring=Right
Sleeve=Ground

USB OTG

I2C Level Translate
For HDMI, maybe DNP



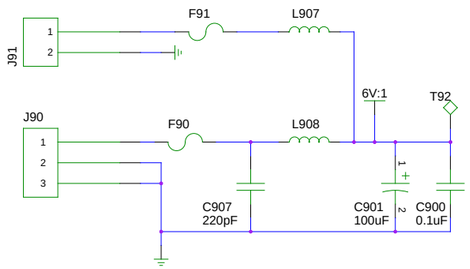
Battery Backup

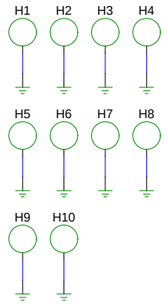
USB Host

USRP Embedded Overo Peripherals

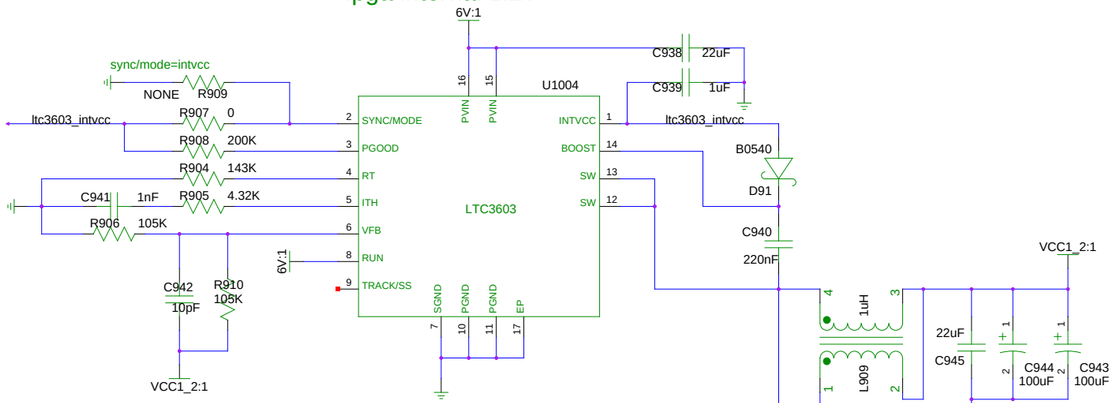
TITLE	$Date$
FILE: overo.sch	REVISION: Rev
PAGE 8 OF 10	DRAWN BY: $Author$

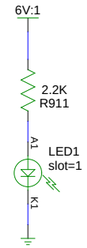
power supply 6v



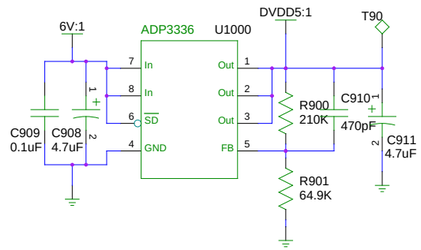


fpga internal 1.2v

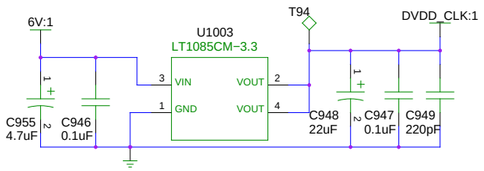




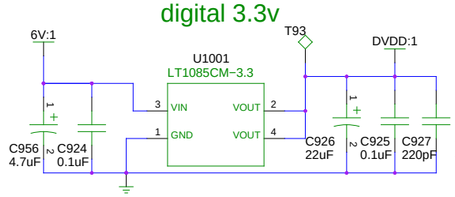
usb host and hdmi connector 5v



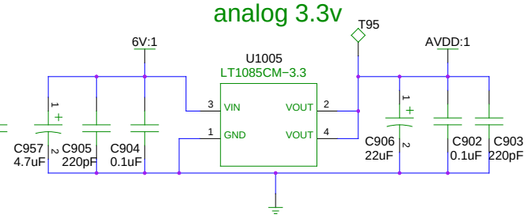
clock 3.3v



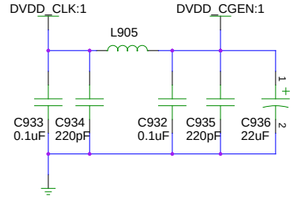
digital 3.3v



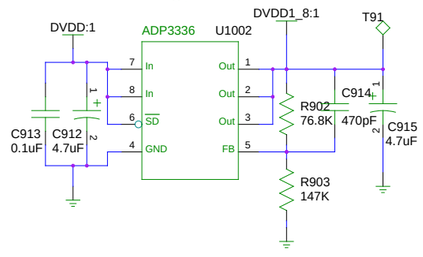
analog 3.3v



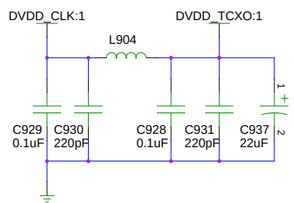
clock gen 3.3v



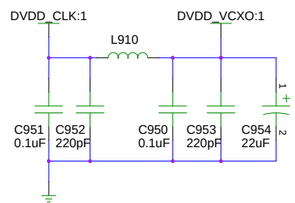
overo gpio 1.8v



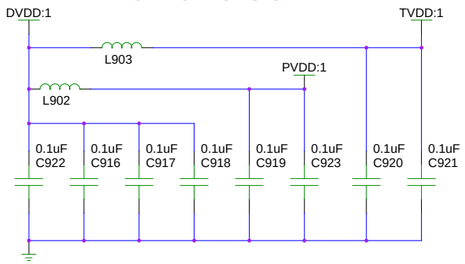
tcxo 3.3v



vcxo 3.3v



hdmi driver 3.3v



USRP Embedded Power Generation

TITLE	$Date$
FILE: power_gen.sch	REVISION: Rev
PAGE 9 OF 10	DRAWN BY: $Author$

USRP Embedded Power Application
TITLE
FILE: power.sch
REVISION: Rev
DRAWN BY: $Author$
$Date$
PAGE 10 OF 10
XC3SD1800ACS484-PWR
U1
DVDD:1
VCC1_2:1
VCCAUX
VCCINT
GND
AD986X-PWR
U400
AVDD
AGND
DVDD
DGND
AVDD:1
DVDD_CODEC:1
L900
C1110
22uF
AD9522-PWR
U100
VS
VCP
GND
DVDD_CGEN:1
DVDD:1
VCC1_2:1
GPS power connector 6v
J101
6V:1
C1167
0.1uF
fan connector 5v
J100
DVDD5:1
L1000
C1063
0.1uF
C1064
0.1uF