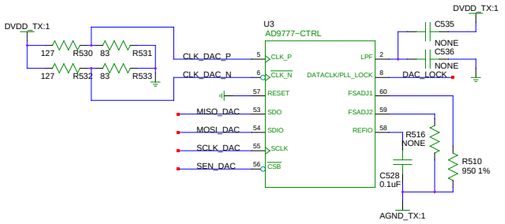
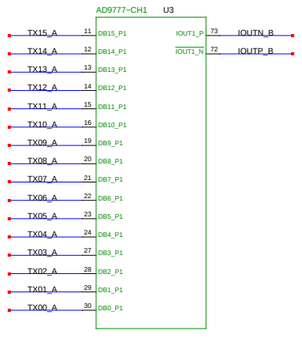
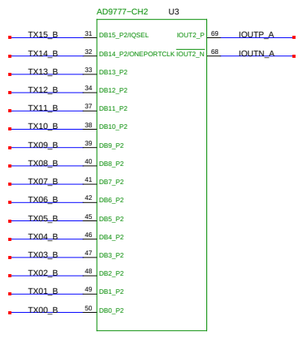
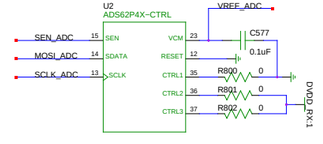
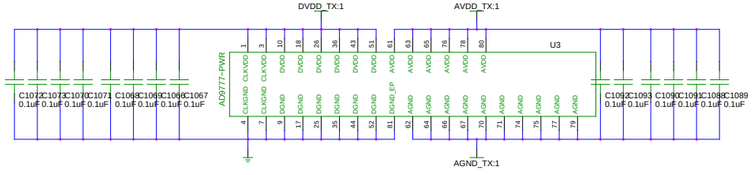
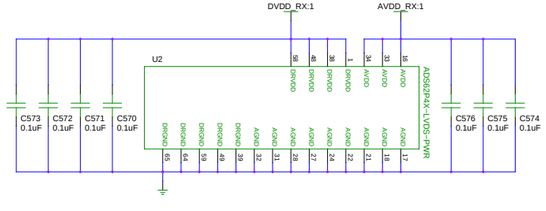












USRP2-Plus CODECs

TITLE	$Date$
FILE: codecs.sch	REVISION: Rev
PAGE 3 OF 12	DRAWN BY: $Author$

USRP2−Plus Configuration

TITLE: $Date$

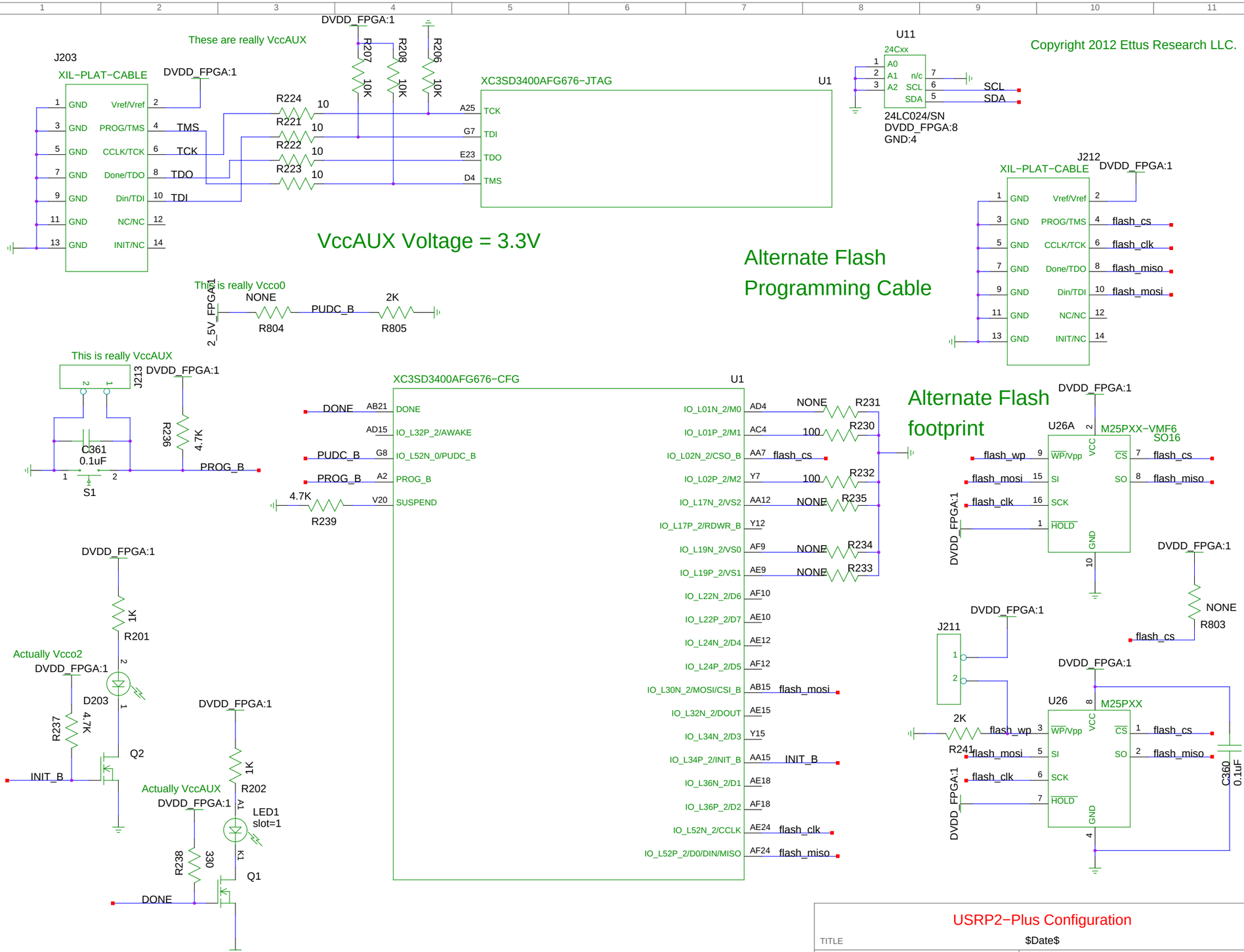
FILE: config.sch | REVISION: $Revision$

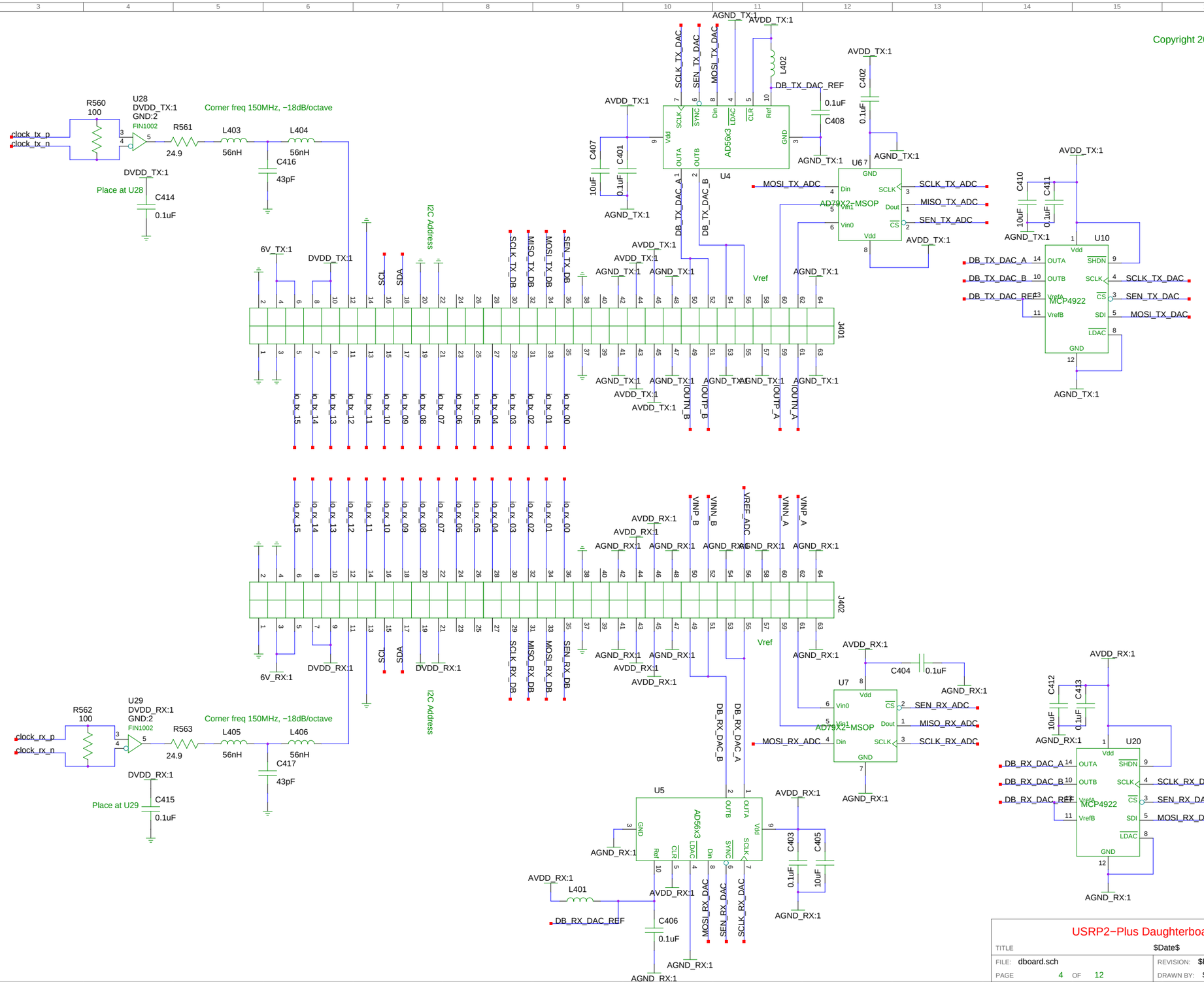
PAGE 2 OF 12 | DRAWN BY: $Author$

VccAUX Voltage = 3.3V

Alternate Flash Programming Cable

Alternate Flash footprint





USRP2−Plus Daughterboad Interface

TITLE	$Date$
FILE: dboard.sch	REVISION: $Revision$
PAGE 4 OF 12	DRAWN BY: $Author$

DB_RX_DAC_A

Outputs to:
DAC −− PECL
ADC −− PECL
FPGA −− PECL
TestCLK −− PECL

Expansion −− LVDS
TX−Dboard −− LVDS
RX−Dboard −− LVDS
SERDES −− LVDS

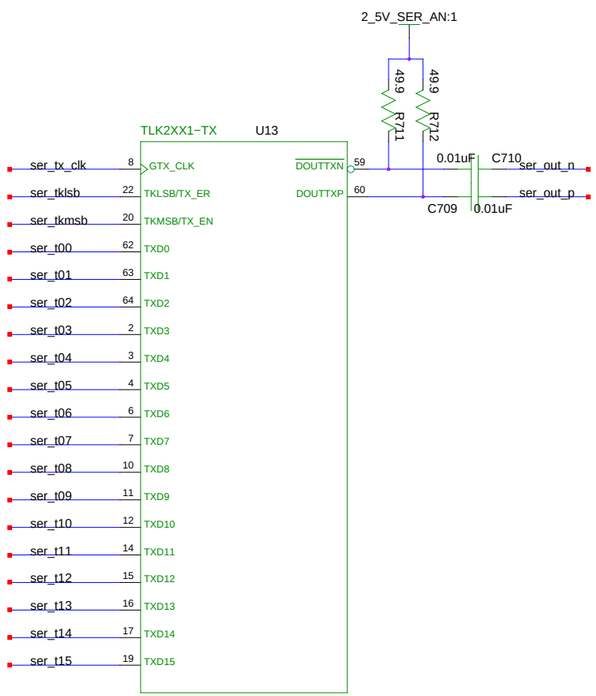
3kHz BW, 45 deg Phase margin
with 5 MHz compare freq and 3mA CP current

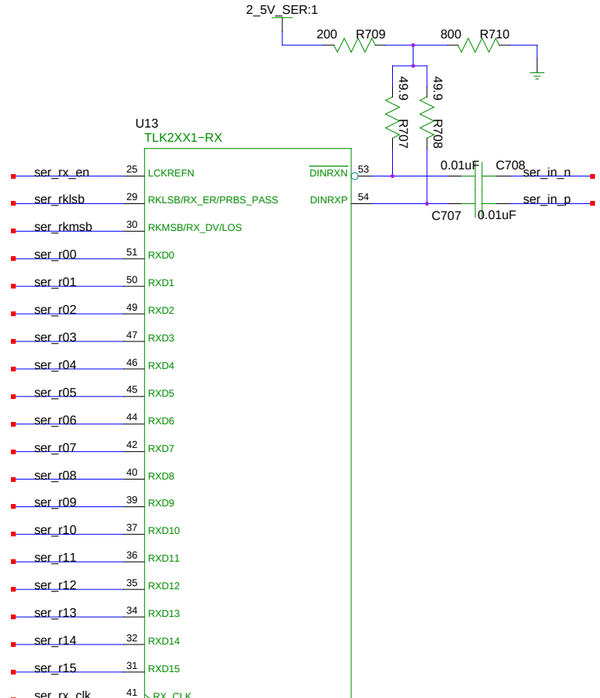
10uF under U8
0.1uF next to pin 4 of U8

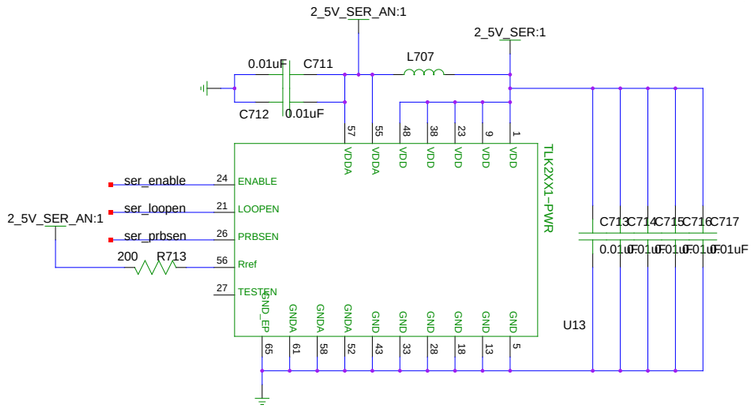
SERDES clk is generated from FPGA

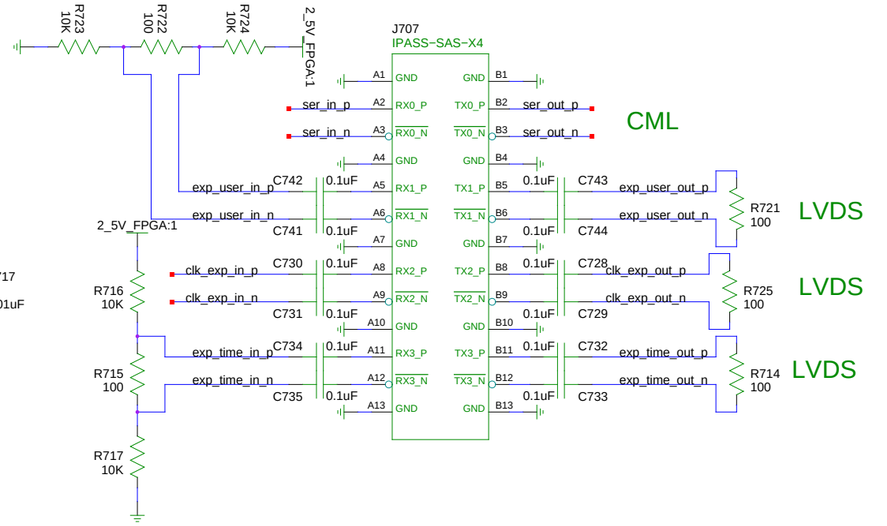
For Firefly GPSDO

TITLE	USRP2−Plus Clocks
	$Date$
FILE: clock.sch	REVISION: Rev
PAGE 5 OF 12	DRAWN BY: $Author$

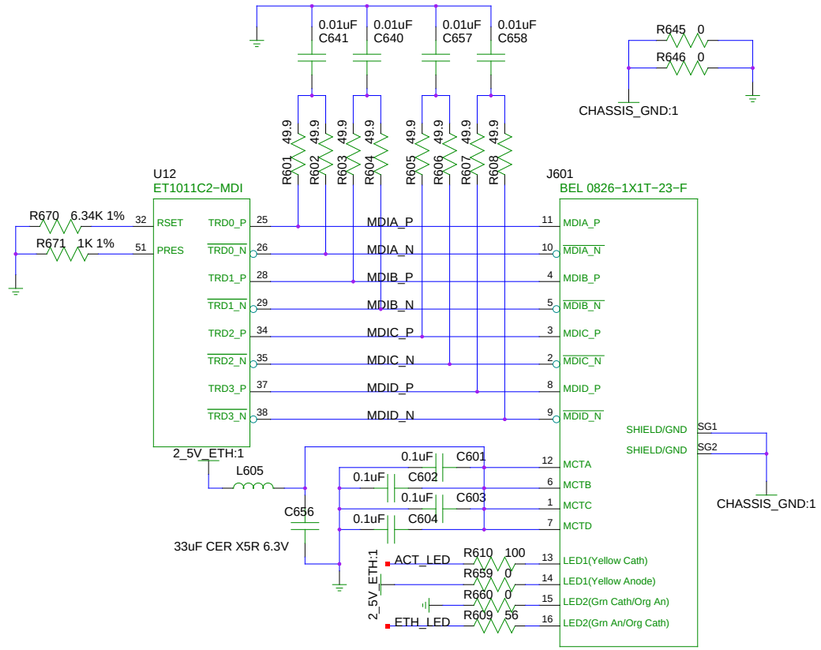


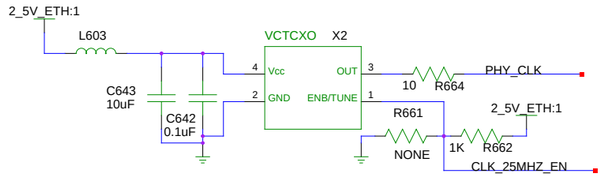


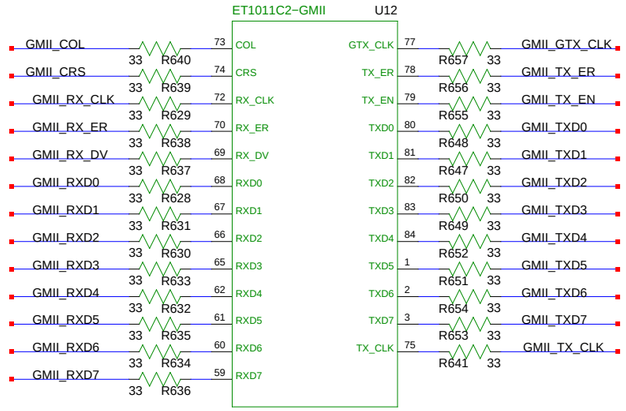


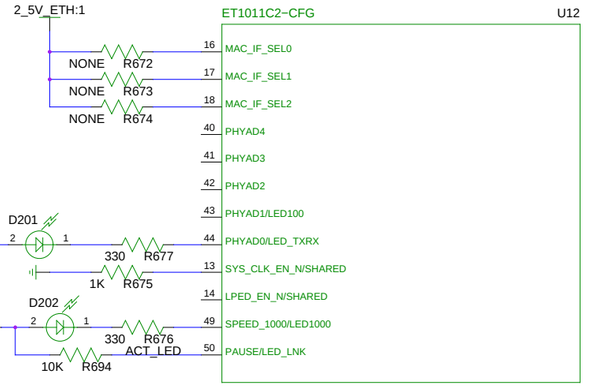


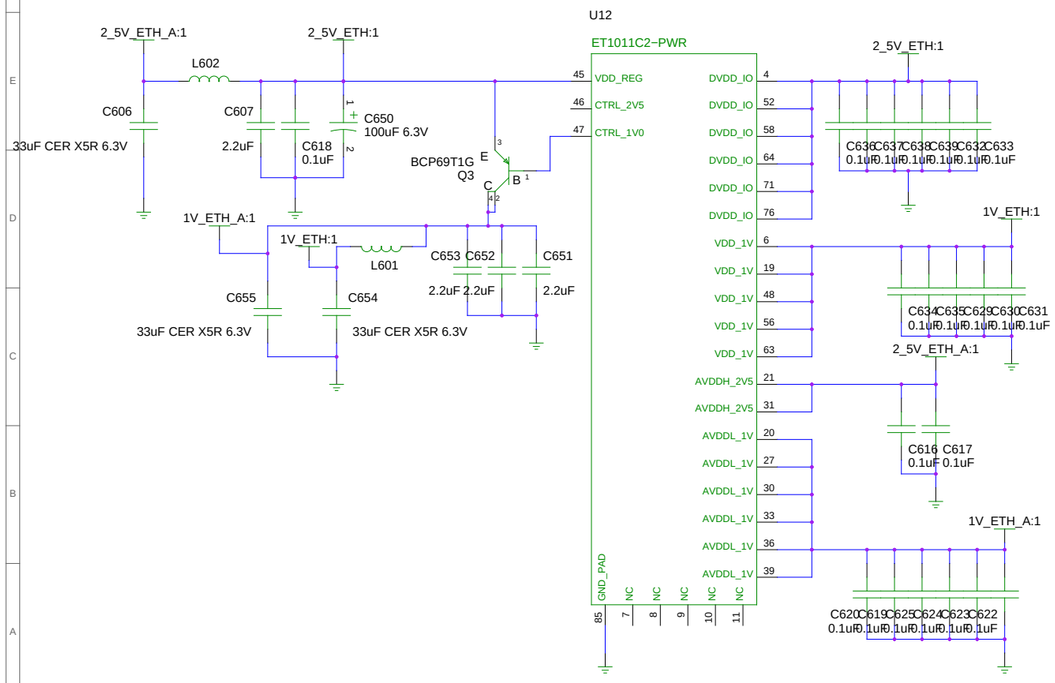
USRP2-Plus Expansion	
TITLE: $Date$	
FILE: expansion.sch	REVISION: $Revision$
PAGE 7 OF 12	DRAWN BY: $Author$

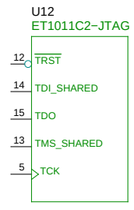


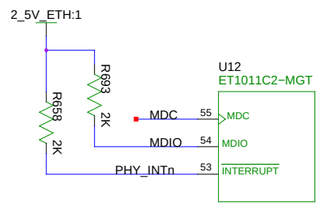


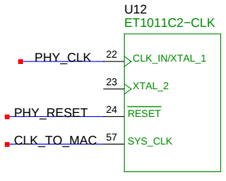






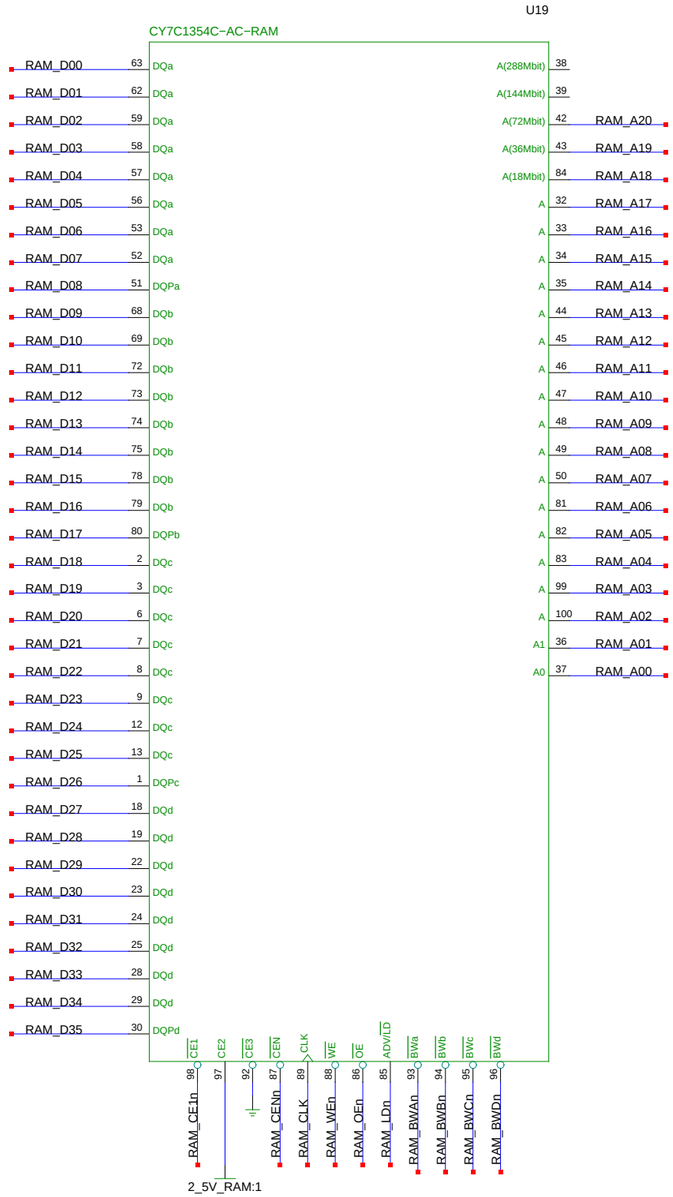




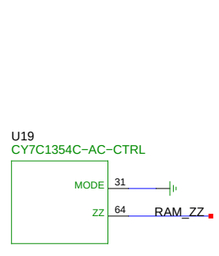


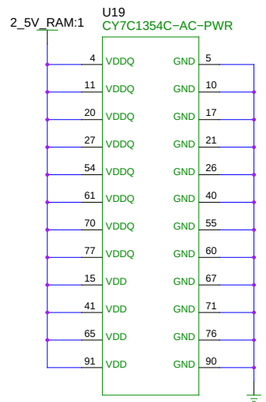
USRP2-Plus Ethernet

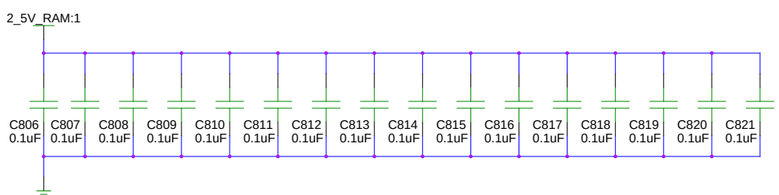
TITLE	$Date$
FILE: ethernet.sch	REVISION: $Revision$
PAGE 6 OF 12	DRAWN BY: $Author$



FIXME −− Extra Power Supply Pins for IDT Version?



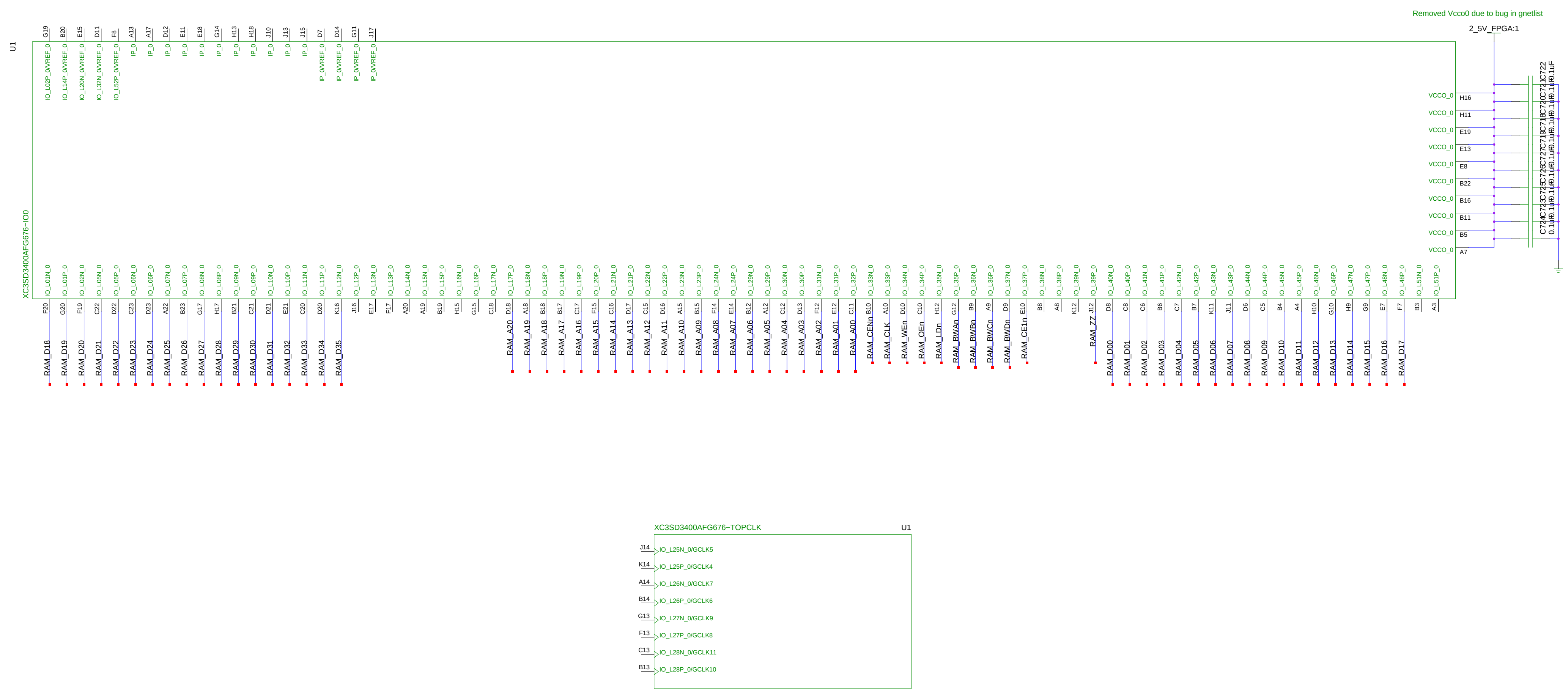




USRP2−Plus RAM

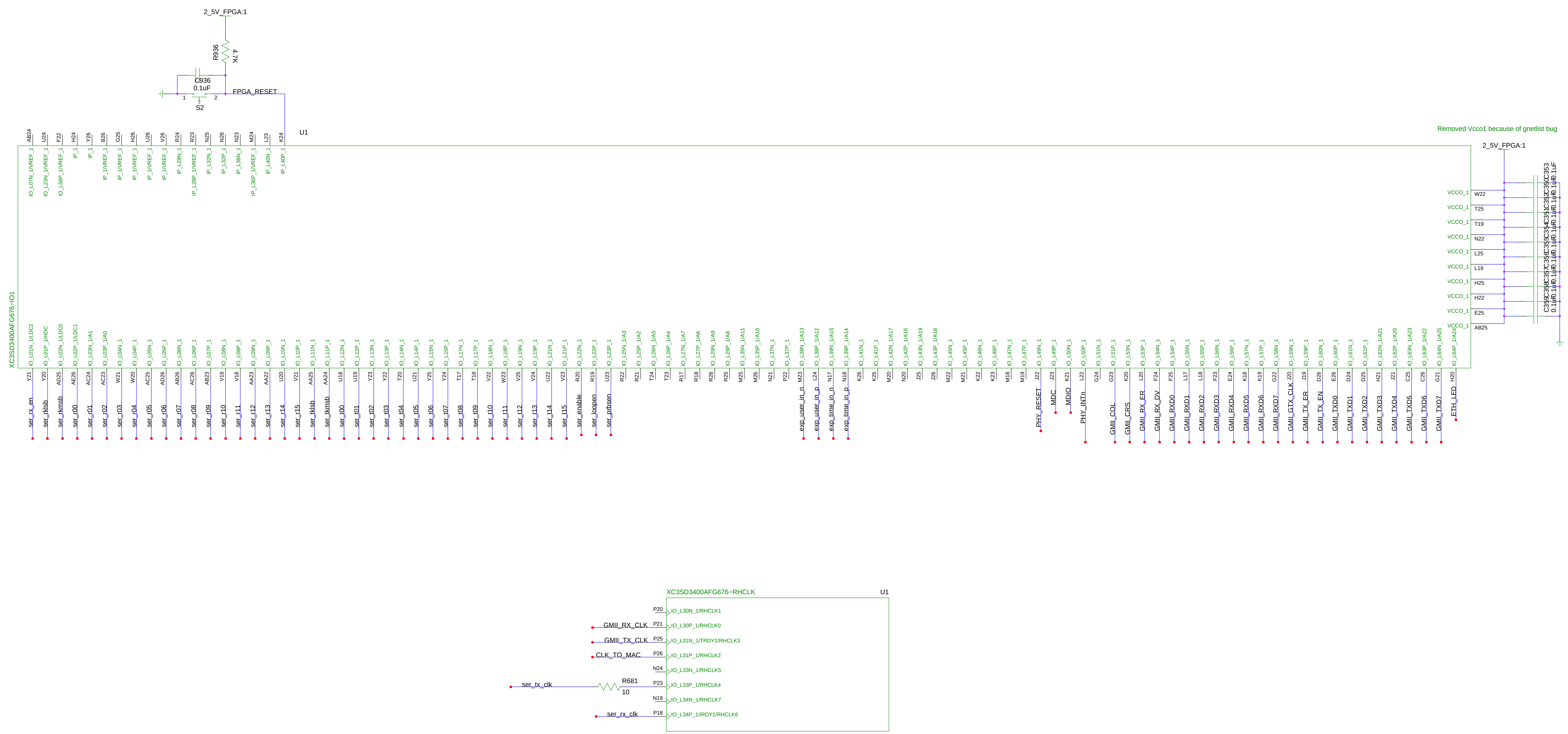
TITLE	$Date$
FILE: ram.sch	REVISION: Rev
PAGE 8 OF 12	DRAWN BY: $Author$

Bank 0, 2.5V
RAM



TITLE	USRP2-Plus FPGA Bank 0
	$Date$
FILE: fpga-bank0.sch	REVISION: Rev
PAGE 9 OF 12	DRAWN BY: $Author$

Bank 1, 2.5V
No LVDS Out
Ethernet
SERDES
Expansion LVDS in



USRP2-Plus FPGA Bank 1			
TITLE	$Date$		
FILE: fpga-bank1.sch		REVISION:	Rev
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Bank 2, 3.3V
SPI Config
Clock Interface
Debug
I2C
BOTCLK
LEDs
RS232

FIXME −−− Do we need RTS, CTS, DTR, DSR, CD, RI?

J301 MICTOR43−LA

J305

L301 DVDD_FPGA:1 DVDD_232:1

C340 0.1uF C342 0.1uF C341 22uF CER X5R 10V

R315 30 R316 30 RXD1 TXD1

U25 MAX232 footprint=SO16 device=MAX3232E

C336 0.1uF C337 0.1uF C338 0.1uF C339 0.1uF

TXD2_232 RXD2_232 TXD3_232 RXD3_232 TXD2 RXD2 TXD3 RXD3

R686 R683 R684 R685 NONE 100

J311 R691 NONE

R690 R687 R688 R689 NONE 0

J312

U1 XC3SD3400AFG676−IO2

Removed Vcco2 because of gnetlist bug

{SEN,MOSI,SCLK}_{TX_DB,TX_DAC,TX_ADC,DAC}
all moved from bank 3 (12 total lines)

R301 2.2K R302 2.2K SCL SDA

LED1 LED2 LED3 LED4 LED5 R311 R312 R314 R313 R682

XC3SD3400AFG676−BOTCLK U1

CLK_FPGA_N CLK_FPGA_P exp_time_out_n exp_time_out_p exp_user_out_n exp_user_out_p

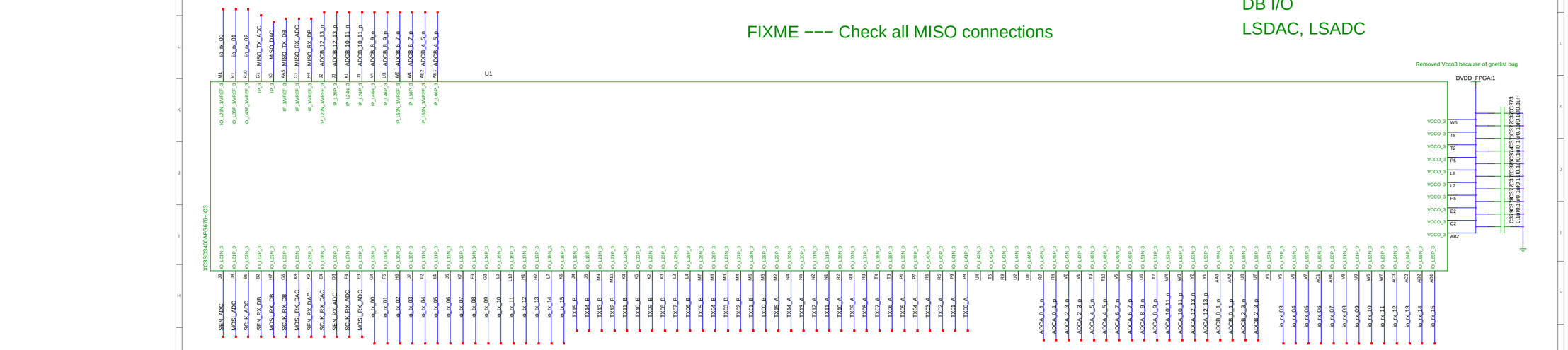
USRP2−Plus FPGA Bank 2

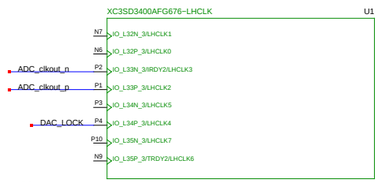
TITLE $Date$ FILE: fpga−bank2.sch REVISION: Rev PAGE 11 OF 12 DRAWN BY: $Author$

Bank 3, 3.3V
DAC
ADC
DB I/O
LSDAC, LSADC

FIXME −−− Check all MISO connections

Removed Vcco3 because of gnetlist bug





{SEN,MOSI,SCLK}_{TX_DB,TX_DAC,TX_ADC,DAC}
all moved to bank 2 (12 total lines)

USRP2−Plus FPGA Bank 3

TITLE:	$Date$
FILE: fpga−bank3.sch	REVISION: Rev
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Front Panel Power

ALT Power

FAN Power

Power Supplies

6V Daughterboard Power (<1A), 5V for clock reg

3.3VCLK AD9510 (<500mA), Clock (88mA)

3.3VAN ADC (200mA), DAC (<500mA)

3.3VDIG All IO (<2A), FPGA AUX

2.5V 1A −− Ethernet Core (600mA), SERDES (<150mA), RAM (<300mA)

1.2V FPGA Core (<2A)

1.0V Ethernet Core

FIXME −− More Decoupling on 1.2 at FPGA

TITLE	USRP2−Plus Power
	$Date$
FILE: power.sch	REVISION: $Revision$
PAGE 1 OF 12	DRAWN BY: $Author$