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# USRP™ N200 & N210 Memory & Certificate of Volatility

This document describes all memory types present on the Ettus Research™ USRP™ N200 series and how to remove all software from the device.

## Memory Types

This section contains information on the memory components used in the USRP N200 series, including details on the size, type, purpose, location, volatility, and the required sanitization procedure.

The device uses both volatile and non-volatile memory types. The volatile memory in the device does not have battery backup and therefore does not retain any information when power is removed. On the other hand, the non-volatile memory requires specific sanitization procedures to clear it of any data.

The following reference table will provide a breakout of the memory types used on the USRP N200 series which currently includes both the USRP N200 and the USRP N210.

| Memory Type & Model | Memory Size | Volatile | Purpose/Contents | Location | Sanitization Procedure |
|---|---|---|---|---|---|
| **SRAM - Cypress**<br>CY7C1354CV25-200AXC or equivalent | 1 Mbit | Yes | Transmit Buffering | U19 | 1 |
| **FPGA - Xilinx**<br>**XC3SD1800A-5FGG676C (N200)**<br>- Configuration Memory<br>- User Memory<br>**XC3SD3400A-5FGG676C (N210)**<br>- Configuration Memory<br>- User Memory | <br><br>8.2 Mbits<br>1.5Mbits<br><br>11.7 Mbits<br>2.2 Mbits | Yes | Configuration and Digital Signal Processing Data | U1 | 1 |
| **Flash Memory - STMicroelectronics**<br>M25P32-VME6P or equivalent<br>M25P64-VME6P or equivalent | 32 Mbits<br>64 Mbits | No | Firmware functions, factory settings. Programming code for the FPGA. | U26, U26A | 2 |
| **EEPROM - Microchip**<br>24LC025 | 2 Kbits | No | Model number, serial number, MAC & IP addresses. Contains no user data. | U11 | 3 |

## Sanitization Procedures

This section contains information on sanitization procedures required to clear all software from the USRP N200 series devices.

**Procedure 1**

Remove power to clear all volatile memory.

**Procedure 2**

Run the following script (available upon request): usrp_n2xx_net_eraser.py

**Procedure 3**

Although the onboard EEPROM can be cleared, it is not necessary as it does not contain any user data.

## Recovery Procedure

Please note that a JTAG programmer will be required to restore the USRP N2X0 to a functional state after executing procedure 2.

The default compiled FPGA image (.bin file) is available on ettus.com as part of the UHD driver distribution or on any computer where the appropriate version of the UHD driver is installed. The path to the .bin image file is:

<UHD install path>\share\uhd\images

A Xilinx FPGA configuration file (.bit file) generated by the Xilinx FPGA design software will also be required. This file can be obtained by compiling the FPGA code distributed by Ettus Research or by requesting the current version from Ettus Research.

In order to load the BIN and BIT files, the following hardware and software are required:

- Xilinx iMPACT software

    The free version will load compiled FPGA code on both the USRP N200 and N210

- Xilinx Platform Cable USB II - Model DLC10

    http://www.xilinx.com/products/boards-and-kits/HW-USB-II-G.htm

Please refer to the documentation provided with Xilinx iMPACT software for details on how to load the files.

Ettus Research will not be held responsible for reprogramming USRP devices that have been cleared using this procedure.